An Efficient Steady-State Simulation of Class-E Resonant Inverter Considering MOSFET Parasitic Components by Using Extended Impedance Method

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***Abstract*—In the previous studies, it has been shown that the steady-state operation of a class-E resonant inverter can be rapidly simulated in the frequency domain by extending the concept and mathematical form of electrical impedance. This paper provides a more comprehensive solution for the efficient simulation of practical class-E resonant inverter, which is driven by a MOSFET switch. The parasitic components, which might influence the operation of the resonant inverter, are taken into consideration in the new equivalent model. These important parasitic components include the linear gate-to-drain capacitance, the nonlinear drain-to-source capacitance, the body diode, etc. The efficient simulation is realized by generalizing the extended impedance method (EIM) to cope with the nonlinearity and multiple-sources problems. Both comparisons to the experimental result and PSpice time-domain simulation show the capability and efficiency of this EIM based solution towards the steady-state simulation of general class-E resonant inverter circuit.**

I. Introduction

Known for its high power conversion efficiency, the class-E resonant inverter, or originally called class-E power amplifier (PA), is an essential building block in modern communication systems [1] and some emerging applications, such as the wireless power transfer [2], [3].

The class-E topology was derived from the conceptual waveforms, which predicted its high power conversion efficiency [4]. Yet, circuit simulation is very important for investigating the actual influence of the parasitic components. Existing time-domain simulator, such as the SPICE, can simulate the actual dynamics of the class-E circuit considering the parasitic components. However, the time-domain method requires going through a useless transient before arriving at the steady-state result. A more efficient circuit simulation method is necessary for directly providing the steady-state operation of class-E PA. Such effort was made by introducing the extended impedance method (EIM) [5], [6].

Previous EIM based analysis has taken the time-varying components [5] and nonlinear components (voltage or current dependent) [6] into consideration. In this paper, the gate drive effect is further broken down into details, which include the gate-drive voltage (signal) source, gate resistance, gate-to-source capacitance, and gate-to-drain capacitance, such that to provide a more comprehensive circuit model towards the efficient simulation of a practical class-E resonant inverter.

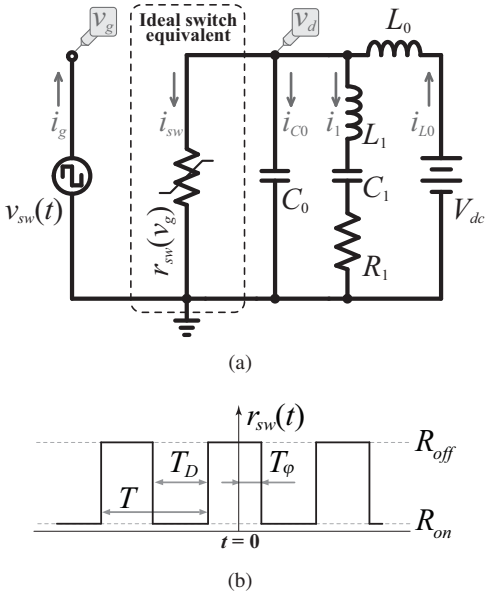

Fig. 1. EIM based analysis for class-E resonant inverter in the previous study [5]. (a) Equivalent model. (b) Switching pattern of $r_{sw}(t)$.

II. EIM Based Class-E PA Analysis [5]

The original EIM based analysis was derived for the steady-state simulation and optimization of class-E resonant inverter with linear components [5]. The equivalent model used in the initial study is shown in Fig. 1(a). In that model, the switching component is ideally taken as a time-varying resistor $r_{sw}(t)$, whose resistance value is determined by the gate drive voltage pulse $v_{sw}(t)$. As the MOSFET gate was regarded open-circuited or to have infinite input impedance, there is no delay between the jumping edges of $v_{sw}(t)$ and the value changing instants of r_{sw}, i.e., the on/off transitions of the transistor; therefore, r_{sw} can be simply regarded as a time-varying resistance, whose switching pattern is shown in Fig. 1(b). By extending the mathematical form of electrical impedance into complex matrix, which describes the cross-frequency relations between the voltage across and current through a time-varying component,

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the class-E circuit dynamics can be summarized as follows

$$\mathbf{Z_{class-E}} = \mathbf{Z_{L0}} + [\mathbf{Z_{sw}}||\mathbf{Z_{C0}}||(\mathbf{Z_{L1}} + \mathbf{Z_{C1}} + \mathbf{Z_{R1}})], \quad (1)$$

where the matrices $\mathbf{Z_{L0}}$, $\mathbf{Z_{sw}}$, $\mathbf{Z_{C0}}$, $\mathbf{Z_{L1}}$, $\mathbf{Z_{C1}}$, and $\mathbf{Z_{R1}}$ correspond to the impedance of L_0, r_{sw}, C_0, L_1, C_1, and R_1 in Fig. 1(a), respectively. The steady-state voltages and currents of any node therefore can be obtained by intuitively applying the conventional series and parallel circuit laws and the Ohm's law. For example, the vector form of the class-E characteristic voltage v_d, whose corresponding node is marked in Fig. 1(a), can be obtained as follows

$$\mathbf{V_d} = [\mathbf{Z_{class-E}} - \mathbf{Z_{L0}}]\,\mathbf{Z_{class-E}^{-1}}\mathbf{V_{dc}}, \quad (2)$$

where $\mathbf{V_{dc}}$ is the corresponding vector of the dc supply V_{dc}. It is composed of the information of its harmonic components. The time-domain waveforms of v_d can be obtained by applying the Fourier series expansion to $\mathbf{V_d}$.

III. Improved EIM Based Analysis Considering Nonlinear Components [6]

The original EIM based analysis can only solve the steady-state performance considering the ideal switch transistor. Yet, recent studies have shown that the parasitic components in a practical MOSFET switch plays a significant role when the class-E PA operates under high frequency [7], [8]. In particular, the nonlinear drain-to-source junction capacitance can serve as the dominant part of the shunt capacitance under high-frequency operation. In a practical MOSFET, the junction capacitance and body diode are voltage-dependent components. For taking the nonlinear components into consideration, the non-iterative EIM algorithm should be further developed into an iterative algorithm. The principle and detailed flow chart concerning the initial and improved EIM based class-E PA design procedures were presented in [6].

The junction capacitance and body diode equivalent resistance are the two nonlinear components that were taken into consideration in the improved EIM based analysis in [6]. These two nonlinear components c_{ds} and r_{bd} connect the drain and source of the MOSFET transistor, as shown in green in the new equivalent model illustrated in Fig. 2. The values of these two components can be expressed as functions of the drain-to-source voltage v_d, i.e.,

$$c_{ds}(v_d) = \begin{cases} C_{j0}\left(1 + \dfrac{v_d}{V_{bi}}\right)^{-m}, & v_d \geq 0; \\ C_{j0}, & v_d < 0. \end{cases} \quad (3)$$

$$r_{bd}(v_d) = \begin{cases} \infty, & v_d \geq 0; \\ -\dfrac{v_d}{I_S\left[e^{-v_d/(nV_T)} - 1\right]}, & v_d < 0. \end{cases} \quad (4)$$

In (3), V_{bi} is the built-in potential of a PN junction; C_{j0} is the zero-bias junction capacitance, i.e., the capacitance when $v_d = 0$; m is the bulk junction grading coefficient typically in the range of 0.3 and 0.4. In (4), I_S is the saturation current; V_T is the thermal voltage; n is the ideal factor.

Since the values of c_{ds} and r_{bd} are functions of the circuit state, they cannot be determined before getting the circuit into operation. Therefore, when nonlinear components are included in the analysis, iterative computation is inevitable towards the steady-state result. By denoting the impedance of c_{ds} and r_{bd} in the (n)th round iteration as $\mathbf{Z_{ds}^{(n)}}$ and $\mathbf{Z_{bd}^{(n)}}$, the improved expression of class-E circuit dynamics can be developed from (1) and provided as follows

$$\mathbf{Z_{class-E}^{(n)}} = \mathbf{Z_{L0}} + \left[\mathbf{Z_{sw}}||\mathbf{Z_{ds}^{(n)}}||\mathbf{Z_{bd}^{(n)}}||\mathbf{Z_{C0}}||(\mathbf{Z_{L1}} + \mathbf{Z_{C1}} + \mathbf{Z_{R1}})\right]. \quad (5)$$

Equation (5), at the same time, also serves as the update function refreshing the equivalent impedance of the class-E circuit between two iterations. The characteristic voltage v_d in the next $(n+1)$th round iteration can be obtained according to the same relation given in (2). i.e.,

$$\mathbf{V_d^{(n+1)}} = \left[\mathbf{Z_{class-E}^{(n)}} - \mathbf{Z_{L0}}\right]\left[\mathbf{Z_{class-E}^{(n)}}\right]^{-1}\mathbf{V_{dc}}. \quad (6)$$

The time-domain expression of $v_d^{(n+1)}(t)$ is obtained from its harmonic vector. Submitting $v_d^{(n+1)}(t)$ into (3) and (4) for making the *state-to-time mapping*, the time-domain expression of c_{ds} and r_{bd} in the $(n+1)$th round, i.e., $c_{ds}^{(n+1)}(t)$ and $r_{bd}^{(n+1)}(t)$, can be derived. The corresponding impedance matrices of these two time-varying components in the $(n+1)$th round can be constructed as $\mathbf{Z_{ds}^{(n+1)}}$ and $\mathbf{Z_{bd}^{(n+1)}}$, based on which the equivalent impedance of the class-E circuit in the $(n+1)$th round, i.e., $\mathbf{Z_{class-E}^{(n+1)}}$, is ready to be obtained based on the update function of (5). The iteration stops when the result satisfies the simulation tolerance [6].

Different from the conventional harmonic balance method [9], which is also a frequency-domain analysis for nonlinear circuits, this EIM based analysis construct the constitutive equations from the component level, rather than from the circuit level differential equations. It approaches the actual solution by numerically update the impedance matrices of the nonlinear components in operation. Solving such EIM based problem does not require conventional numerical solvers, such as the Newton's method. The convergent speed of this EIM algorithm is quite fast and almost guaranteed in previous case studies [6]. Yet, more rigorous mathematics should be applied to further refine and accelerate the numerical process of EIM in the future.

IV. A More Comprehensive EIM Based Analysis Considering the Gate-Drive Effect

The initial EIM based class-E PA analysis has incorporated the time-varying component in the impedance based circuit analysis [5]; while the improved EIM based analysis has involved the nonlinear components in the impedance network [6], and therefore generalized the EIM for the nonlinear circuit simulation. Nevertheless, the previous two studies have considered simple impedance networks, which are constructed by only parallel and series connections and have only one driven source. A more general network might have more complex connection, such as the Y or Δ connections in the three-phase circuits, and might also have multiple sources as

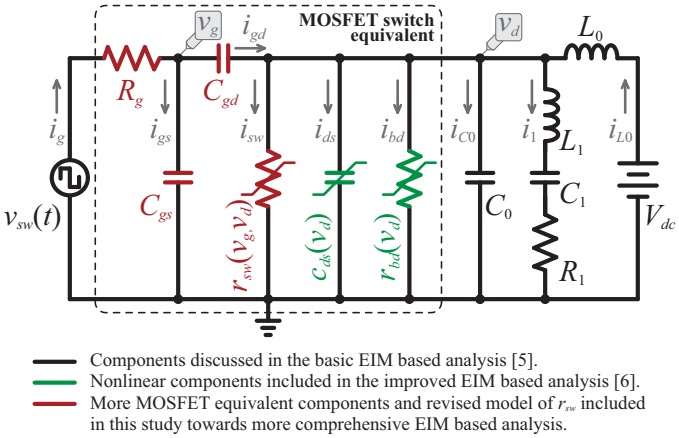

Fig. 2. Equivalent model of the class-E resonant inverter including the MOSFET parasitic components.

well. The EIM based analysis should be further generalized to cover all these complex circuit networks.

On the other hand, in the study of practical class-E resonant inverter, which is driven by MOSFET, besides the influence of nonlinear parasitic components, the gate-drive voltage might also affect the circuit dynamics through a linear gate-to-drain capacitance C_{gd} [7]. In order to consider the gate drive effect, a more complete model is built and shown in Fig. 2 by referring to the MOSFET parasitic model. The newly added components, compared to [6], are colorized in red in Fig. 2. They include the gate-to-drain capacitance C_{gd}, the gate-to-source capacitance C_{gs}, the gate resistance R_g, and the equivalent switching resistance r_{sw}.

By taking the new equivalent model, the single source impedance networks that used in [5], [6] is changed into a double sources impedance network, whose solution was never discussed in the previous EIM based studies. Moreover, compared to the previous EIM solutions, there is a remarkable revision on the switching resistance r_{sw} in the new equivalent model. In the previous study, the gate-drive voltage is disconnected from the main circuit, or considering infinite gate impedance; therefore, r_{sw} can be simply taken as a time-dependent resistance. Yet, in this study, r_{sw} is considered as another nonlinear component, whose value is determined by both the gate and drain voltages. The mathematical formula of this resistance can be derived according to the MOSFET output characteristics, i.e., the functional relation between the drain-to-source voltage v_d and drain current i_d under different gate voltage v_g. The value of such equivalent resistance can be formulated as follows

$$r_{sw}(v_g,v_d)=\begin{cases} R_{off}, & \text{for } v_g \le V_{th};\\ R_{on}+\dfrac{2L}{\mu_n C_{ox} W\left[2(v_g-V_{th})-v_d\right]}, & \text{for } v_g > V_{th} \text{ and } v_d < v_g - V_{th};\\ R_{on}+\dfrac{2Lv_d}{\mu_n C_{ox} W(v_g-V_{th})^2}, & \text{for } v_g > V_{th} \text{ and } v_d \ge v_g - V_{th}, \end{cases} \quad (7)$$

where the three piecewise expressions correspond to the cutoff, linear region, and saturation region of the MOSFET. Those constants R_{on}, R_{off}, $\mu_n C_{ox}$, W, L, V_{th} in (7) refer to the combination of source and drain ohmic resistance, drain-to-source shunt resistance, transconductance parameter, channel width, channel length, and zero-bias threshold voltage, which can be looked up from the SPICE component library [7].

As mentioned, an additional issue that has been brought in by the new model is that there are two independent voltage sources, i.e., the gate-drive voltage $v_{sw}(t)$ and dc supply V_{dc}, which together influence the circuit dynamics. In this case, the network relation can no longer be expressed with the simple series and parallel laws. It should be analyzed with the more comprehensive Kirchhoffś circuit laws. The constitutive matrix is built according to the KVL and KCL, and it is expressed as follows

$$\begin{bmatrix} \mathbf{V_{sw}} \\ \mathbf{V_{dc}} \\ \mathbf{0} \\ \mathbf{0} \\ \mathbf{0} \end{bmatrix} = \begin{bmatrix} \mathbf{Z_g} & \mathbf{Z_{gs}} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{Z}_{\Sigma}^{(n)} & \mathbf{Z_{L0}} \\ \mathbf{0} & \mathbf{Z_{gs}} & -\mathbf{Z_{gd}} & -\mathbf{Z}_{\Sigma}^{(n)} & \mathbf{0} \\ \mathbf{1} & -\mathbf{1} & -\mathbf{1} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{1} & -\mathbf{1} & \mathbf{1} \end{bmatrix} \begin{bmatrix} \mathbf{I}_{\mathbf{g}}^{(n+1)} \\ \mathbf{I}_{\mathbf{gs}}^{(n+1)} \\ \mathbf{I}_{\mathbf{gd}}^{(n+1)} \\ \mathbf{I}_{\Sigma}^{(n+1)} \\ \mathbf{I}_{\mathbf{L0}}^{(n+1)} \end{bmatrix}, \quad (8)$$

where

$$\mathbf{Z}_{\Sigma}^{(n)} = \mathbf{Z}_{\mathbf{sw}}^{(n)} \,\|\, \mathbf{Z}_{\mathbf{ds}}^{(n)} \,\|\, \mathbf{Z}_{\mathbf{bd}}^{(n)} \,\|\, \mathbf{Z_{C0}} \,\|\, (\mathbf{Z_{L1}} + \mathbf{Z_{C1}} + \mathbf{Z_{R1}}); \quad (9)$$

$$\mathbf{I}_{\Sigma}^{(n+1)} = \mathbf{I}_{\mathbf{sw}}^{(n+1)} + \mathbf{I}_{\mathbf{ds}}^{(n+1)} + \mathbf{I}_{\mathbf{bd}}^{(n+1)} + \mathbf{I}_{\mathbf{C0}}^{(n+1)} + \mathbf{I}_{\mathbf{1}}^{(n+1)}. \quad (10)$$

In (8), $\mathbf{1}$ and $\mathbf{0}$ denotes the identity and zero matrices; $\mathbf{Z_g}$, $\mathbf{Z_{gs}}$, and $\mathbf{Z_{gd}}$ denote the impedance of R_g, C_{gs}, and C_{gd}, respectively. The dimension of the matrix in (8) is $[5\times(2K+1)]^2$, where K is the number of the included harmonics. The superscript (n) in (8)–(10) denotes that it is the result or parameter in the (n)th round calculation.

Substituting (9) into (8) and solving the linear equations give the operating currents and voltages in the $(n+1)$th round. According to (7), (3), and (4), the information of gate-to-source and drain-to-source voltages in the $(n+1)$th round, i.e., $v_g^{(n+1)}(t)$ and $v_d^{(n+1)}(t)$ can be used to derive the values of the three nonlinear components in the same round of calculation, i.e., $r_{sw}^{(n+1)}(t)$, $c_{ds}^{(n+1)}(t)$, and $r_{bd}^{(n+1)}(t)$. These time-varying functions lead to their corresponding frequency-domain expressions $\mathbf{Z}_{\mathbf{sw}}^{(n+1)}$, $\mathbf{Z}_{\mathbf{ds}}^{(n+1)}$, and $\mathbf{Z}_{\mathbf{bd}}^{(n+1)}$, in terms of impedance. Those impedance expressions can be resubmitted into (9) and (8) for starting another round of calculation. The iteration stops when the error is small enough within the preset tolerance [6].

V. Case Studies and Results

Two case studies are carried out considering a single-ended class-E resonant inverter circuit driven by an IRF510 NMOS power transistor with two different square-wave or sinusoidal gate-drive signals (voltages), respectively. The SPICE model of IRF510 has been introduced and used in [7]. The simulated results obtained with the comprehensive EIM is compared with those obtained with the PSpice (Cadence Inc.), one of the

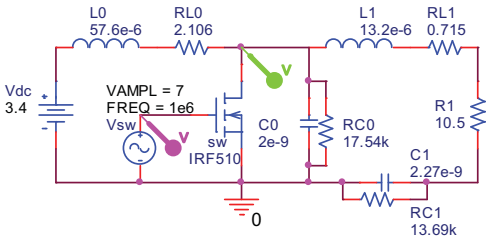

Fig. 3. Simulation circuit built in PSpice for comparative study.

TABLE I
MEASURED PARAMETERS IN THE CASE STUDIES OF CLASS-E PA.

Parameter	Value	ESR / EPR	Value
V_{dc}	3.4 V	–	–
V_{sw} [amp. of $v_{sw}(t)$]	±7.0 V	–	–
f_{sw} [freq. of $v_{sw}(t)$]	1 MHz	–	–
D	50 %	–	–
L_0	57.6 μH	R_{L0}	2.106 Ω
C_0	2.0 nF	R_{C0}	17.54 kΩ
L_1	13.2 μH	R_{L1}	0.715 Ω
C_1	2.27 nF	R_{C1}	13.69 kΩ
R_1	10.5 Ω	–	–
Q	7.90	–	–

The circuit parameters are firstly estimated based on the revised design equations in [10]. Actual component values and their equivalent series resistance (ESR) or equivalent parallel resistance (EPR) provided in this table are obtained from experimental measurement.

TABLE II
PARASITIC PARAMETERS OF POWER MOSFET IRF510.

Parameter	Aliases in SPICE	Value
R_{on}	Rd+Rs	0.47 Ω
R_{off}	Rds	444.4 kΩ
R_g	Rg	2.977 Ω
C_{gs}	Cgso × W	600.5 pF/m × W
C_{gd}	Cgdo × W	62.71 pF/m × W
W	W	0.64 m
L	L	2 μm
V_{th}	Vto	3.697 V
$\mu_n C_{ox}$	Kp	20.68 μA/V^2
C_{j0}	Cbd	366.5 pF
V_{bi}	Pb	0.8 V
m	Mj	0.5
I_S	Is	202.9 fA
n	N	1
V_t	–	26 mV

The parameters are extracted from the SPICE level 3 model of IRF510.

commercialized versions of the prevailing circuit simulator SPICE based on the time-domain technology. Experimental results obtained from real circuit experiment are also provided in this section for the comparative study.

Fig. 3 shows the circuit topology used in the PSpice simulation. Table I provides the detailed circuit parameters, which are measured from the experimental circuit. Those measured parameters are used in both the EIM and PSpice simulations to mimic the practical circuit conditions. Table II provides the values of the parasitic components in IRF510. The MOSFET model is well established as the fundamental knowledge in

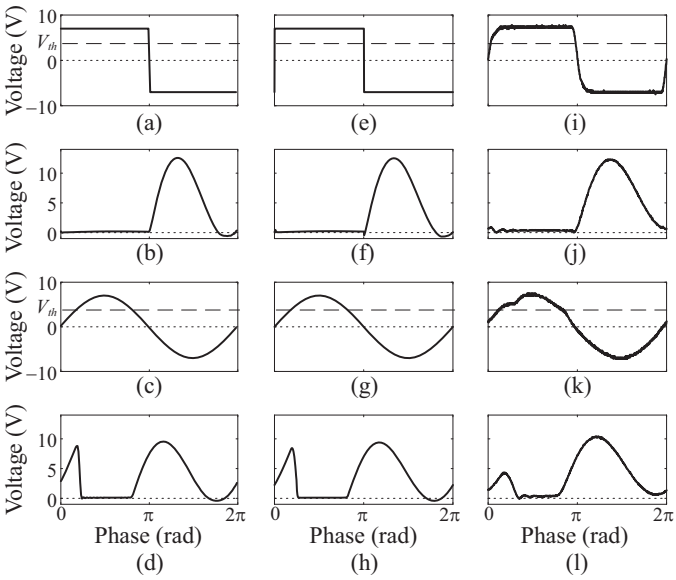

Fig. 4. Comparison among results of EIM simulation (K = 50), PSpice simulation ($\Delta t \leq 1$ ns), and experiment. (a)–(d) EIM. (e)–(h) PSpice. (i)–(l) Experiment. (a), (e), and (i) Square-wave gate-drive voltages v_{sw} and threshold voltage V_{th}. (b), (f), and (j) Drain voltages v_d under square-wave gate-drive voltage. (c), (g), and (k) Sinusoidal gate-drive voltages v_{sw} and threshold voltage V_{th}. (d), (h), and (l) Drain voltages v_d under sinusoidal gate-drive voltage.

analog integrated circuit. Since SPICE is a simulation program with integrated circuit emphasis, those parasitic parameters therefore can be extracted from the model library of PSpice.

The selected harmonic number influences the simulation accuracy in the EIM based frequency-domain simulation; while the time step size matters in the SPICE based time-domain simulation. In these case studies, the harmonic number is set to K = 50 in the EIM simulation; the maximum step size is set to 1 ns in the PSpice simulation. Fig. 4 shows the results of the characteristic drain voltage v_d under the square-wave and sinusoidal gate drive voltages in the EIM, PSpice, and experiment, respectively. The result shows that the EIM result matches the PSpice one quite well. They can both effectively predict the actual waveform of the real circuit. The small discrepancy between simulation and experiment are due to the imperfection of the driving voltages in experiment, which is simply provided by a DC to 25 MHz arbitrary waveform function generator. In particular, the imperfect driving voltages make the MOSFET in experiment turns on slower than the ideal case, as observed from Fig. 4(l); on the other hand, the actual duty cycle in experiment are a little bit smaller than that in the idea case. These problem can be improved in the future by enhancing the driving capability of the gate-drive voltage source.

To further analyze the details of the EIM based simulation of class-E PA under different gate-drive voltages, Fig. 5(a)–(c) and Fig. 6(a)–(c) show the values of nonlinear components at different phase. From Fig. 5(a) and Fig. 6(a), we can observe that the junction capacitance c_{ds} has a big change due to the variation of drain voltage v_d during operation.

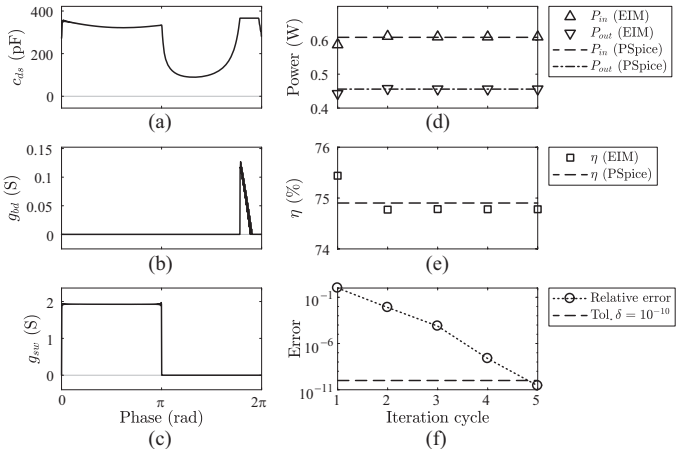

Fig. 5. Results with square-wave gate-drive voltage. (a) Nonlinear junction capacitance c_{ds}. (b) Body diode conductance g_{bd}. (c) Switch conductance g_{sw}. (d) Input and output powers. (e) Conversion efficiency. (f) Relative errors in iteration.

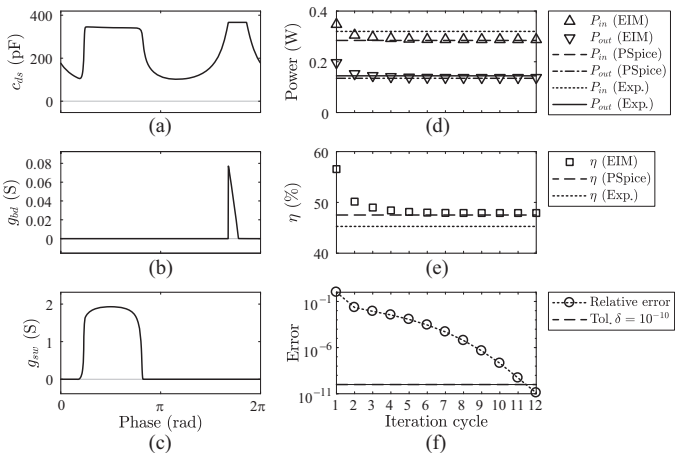

Fig. 6. Results with sinusoidal gate-drive voltage. (a) Nonlinear junction capacitance c_{ds}. (b) Body diode conductance g_{bd}. (c) Switch conductance g_{sw}. (d) Input and output powers. (e) Conversion efficiency. (f) Relative errors in iteration.

From 5(b) and Fig. 6(b), we can observe that the body diode conducts for a short interval before the MOSFET turn-on instants in both cases, because the circuit is not well tuned to operate under the nominal class-E conditions. Since this study is not about the design and optimization of class-E PA, the simulation credibility in general off-nominal operation condition matters more than achieving nominal operation here. From Fig. 5(c), the square-wave driven MOSFET almost gives a perfect switching function, which was assumed in the initial EIM based class-E PA simulation [5]; while from Fig. 6(c) the switch conductance does not has the steep edges, which implies that more power might be lost during the slowly turning on or off in every cycle.

Fig. 5(d) and Fig. 6(d) compare the input and output powers, which Fig. 5(e) and Fig. 6(e) compare the power conversion efficiency in both cases. The EIM result approaches the PSpice one quite well. Since the sinusoidal case seriously violate the ZVS (zero voltage switching) condition, the conversion efficiency is much lower than the square-wave driven case. The experimental results of the input and output powers and efficiency in the sinusoidal case are also provided in Fig. 6(d) and (e). Due to the slow turn-on actions, as observed from Fig 4(l), the conversion efficiency in experiment is a little bit lower than that in simulations.

Fig. 5(f) and Fig. 6(f) show the relative error in both cases. They show that both cases converge very fast and terminated after a few iterations when the relative error is below the tolerance $\delta = 10^{-10}$ (expression can be found in [6]).

VI. Conclusion

Owning to its high power conversion efficiency and simple configuration, the class-E resonant inverter is extensively used in some existing and emerging applications for making the dc-to-ac power conversion. Big efforts have been made on resonance tuning for practical class-E circuit in literature. Efficient simulation tool can help shorten the design procedure and facilitate the optimization or even in-situ tuning. This paper presents an efficient simulation for the class-E circuit based on a more comprehensive version of extended impedance method (EIM). By extending the concept and mathematical form of electrical impedance and improving the algorithm, the EIM can be used to analyze the class-E circuit with a full consideration of the parasitic effect of a MOSFET switch, which is driven by different types of gate-drive voltages. Such EIM based simulation takes much less computational effort compared to the prevailing time-domain circuit simulator towards the useful steady-state results.

In general, the EIM provides a credible alternative simulation solution to the existing methodologies, in particular, with an emphasis on efficient steady-state analysis. It is a promising technology; yet, more effort should be taken on nonlinear component modeling, algorithm improvement, etc. before arriving at a universal EIM tool for the analysis of arbitrary power circuits and systems.

VII. Acknowledgment

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