Parallel Synchronized Septuple Bias-Flip Circuit for Piezoelectric Energy Harvesting Enhancement

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***Abstract*—Literature has shown that the interface circuit plays an important role in a piezoelectric energy harvesting (PEH) system. By referring to the general model of synchronized multiple bias-flip (SMBF) and the recent implementation of parallel synchronized triple bias-flip (P-S3BF), this paper introduces a new implementation called *parallel synchronized septuple bias-flip* (P-S7BF) for further enhancing the PEH performance. By sophisticatedly designing the current steering network, P-S7BF realizes seven self-adaptive voltage bias-flip actions at every synchronized instant, such that it can further increase the net harvested power under the compromise of larger power extraction and smaller dissipation in power conditioning. The steady-state operation of P-S7BF is discussed in detail. Experiments are carried out on a prototyped piezoelectric structure under the same harmonic base vibration. The experimental results show that the ratios among the maximum harvested powers by using P-S7BF, P-S3BF, P-SSHI (parallel synchronized switch harvesting on inductor), and SEH (standard energy harvesting bridge rectifier) are 1.75 : 1.56 : 1.45 : 1.0, which validate the advantage of P-S7BF over the state-of-the-art solutions.**

***Index Terms*—vibration, energy harvesting, piezoelectricity, synchronized bias-flip, ac-dc power conversion.**

I. Introduction

Owing to the technical innovations on high-performance and low-power embedded processors, sensors, wireless communication, etc., the wireless sensor networks (WSN) and Internet of Things (IoT) have become more popular over the last decade. These autonomous electronic devices are usually dispersively distributed. Nowadays, most of them are powered by batteries, whose energy storage are limited. Compared to other technologies that enable pervasive computing, the improvement of batteries was relatively slow [1]. The power supply issue has become one of the biggest constraints for the massive deployment and good maintenance of the distributed electronics [2]. Besides the energy-saving solution, which cuts down the energy consumption towards longer battery life [3], an everlasting power solution is to equip the distributed devices with the self-powering feature, so that they can scavenge energy by themselves from the ambiance [4]. The transducers play an important role in transforming energy with different physical forms into electricity. Piezoelectric, electromagnetic, and electrostatic transducers are three often used electromechanical transducers for energy harvesting from ambient vibrations. Within these three transducers, the piezoelectric one is relatively simple in mechanical configuration. Its output voltage is relatively high and easy to process.

A piezoelectric transducer generates ac voltage in vibration. However, since digital electronics should be powered by dc source, an ac-dc power conversion is necessary as the first stage of power conditioning. The full-wave bridge rectifier, which is the most accessible ac-dc conversion circuit, is regarded as the standard energy harvesting (SEH) interface circuit for piezoelectric energy harvesting (PEH) [5]. After SEH, some synchronized switch solutions were proposed for enhancing the PEH capability. The most extensively investigated circuit solutions are the synchronized switch harvesting on inductor (SSHI) [5], which is also named the bias-flip rectifier in the IC research community [6]. In SSHI, an inductive switching branch is connected to the piezoelectric element. They form an switching LC resonant circuit, which enables a rapid voltage zero-crossing change whenever the piezoelectric current (proportional to the vibration velocity) crosses zero. By using SSHI, the harvested power can be increased by several times under the same vibration excitation [5]. In SSHI, there is only one bias-flip action in each synchronized instant. After that, some synchronized double bias-flip (S2BF) and synchronized triple bias-flip (S3BF) solutions have further refreshed the record of PEH capability by carrying out double and triple bias-flip actions, respectively, at the synchronized instants [7]–[10]. Liang has summarized the working principles of the aforementioned circuits under the theoretical synchronized multiple bias-flip (SMBF) model [11].

Based on existing bias-flip solutions and the theoretical guidance of the SMBF model, this paper introduces the new implementation of the parallel synchronized septuple bias-flip (P-S7BF) circuit. The achievement is realized by sophisticatedly designing the current steering network, which is composed of two auxiliary capacitors for providing the self-adaptive bias voltages, and the switch network, which is composed of 12 transistors and six diodes for regulating the current flow. In this paper, the design and operation of P-S7BF, including its circuit topology, switching sequence, its steady-state and transient behaviors are discussed.

II. SMBF Model [11]

The idea of P-S7BF is originated from the SMBF model, which conceptually generalizes the operation of multiple bias-flip interface circuits, and the optimal bias-flip (OBF) strategy, which aims at getting the maximum net harvested power by

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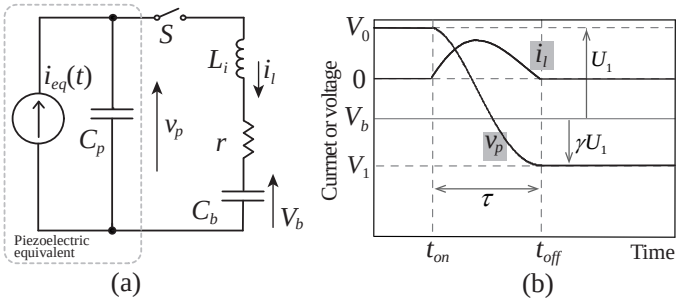


Fig. 1. The principle of a signal bias-flip action. (a) Equivalent circuit. (b) Voltage and current waveforms at a bias-flip instant.

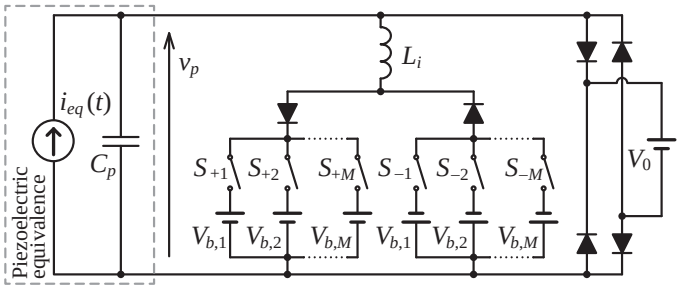


Fig. 2. Conceptual SMBF interface circuit [11].

making the compromise between large extraction and small dissipation under a specific number of bias-flip actions [11].

The bias-flip action is the essential ingredient towards the SMBF solutions, no matter the inductive branch is connected to the transducer in series or parallel, or how many flipping steps are carried out. Given that the response of an electrical circuit is much faster than that of a mechanical structure, in general, the piezoelectric voltage can be instantaneously and electrically manipulated before the mechanical structure makes a response. Fig. 1 shows the principle and current and voltage waveforms of a single bias-flip action based on the piezoelectric equivalent model. The resonant circuit branch realizing a bias-flip action is composed of five elements: the piezoelectric clamped capacitance C_p, an active switch S, an external inductor L_i, the equivalent series resistance (ESR) r, and the auxiliary capacitor C_b. Since C_b is designed to be much larger than C_p, V_b the voltage across C_b is regarded constant during each bias-flip action. The switch resonant circuit formed by these five elements are shown in Fig. 1(a). The waveforms, which are shown in Fig. 1(b), illustrate how the bias flip works by turning on and turning off S at the t_{on} and t_{off} instants, respectively, such that to enable a step transient and instantaneously change of v_p. The switch-on interval of S is fixed and given as follows

$$\tau = t_{off} - t_{on} = \pi\sqrt{L_i C_p}. \tag{1}$$

τ is half of an LC cycle, which enables the maximum change of v_p in a single bias-flip action.

The *flipping factor* γ, which is also called *inversion factor* in literature, defines the voltage change ratio after the voltage manipulation with respect to the referenced bias voltage, as shown in Fig. 1(b). γ is related to the qualify factor Q of the C_p-S-L_i-r-C_b circuit, i.e.,

$$\gamma \triangleq \frac{V_1 - V_b}{V_0 - V_b} = -e^{-\pi/(2Q)}. \tag{2}$$

Given the near constant V_b, because $C_b \gg C_p$, the energy absorbed by the auxiliary capacitor C_b in one bias-flip action can be expressed as follows

$$\Delta E_b = \Delta Q V_b = C_p(1-\gamma)U_1 V_b, \tag{3}$$

where $U_1 = V_0 - V_b$ as shown in Fig. 1(b). The SSHI solutions use a single passive bias-flip (energy absorbing) action for PEH enhancement [5], where $\Delta E_b \geq 0$. Latter solutions introduce the active (energy investing) actions [7]–[9] to the system, where $\Delta E_b < 0$. The energy relation, therefore, has become more complicated for balancing the positive and negative E_b towards maximum net harvested power.

Fig. 2 shows the parallel version of the conceptual SMBF model. The multiple bias-flip actions in each synchronized instant are carried out by successively conducting half of the switch branches containing S_{+m} ($m = 1, 2, ..., M$), or those containing S_{-m}. Summing up the energy income (positive for absorption and negative for investment) of all $2M + 1$ sources, the net harvested energy in one cycle can be obtained as follows

$$E_{h,net} = 2\left(\sum_{m=1}^{M} \Delta E_{b,m} + \Delta E_p\right). \tag{4}$$

ΔE_p is the energy absorbed by V_0 in the parallel bridge rectifier in a half cycle, i.e.,

$$\Delta E_p = C_p V_0 (V_{oc} - V_0 - V_M), \tag{5}$$

where V_{oc} is the equivalent open-circuit voltage; V_M is the final voltage after M bias-flip actions in a synchronized instant.

The maximum $E_{h,net}$ is obtained under a set of optimal bias voltages $V_{b,m}$ ($m = 1, 2, ..., M$). Liang [11] has defined the non-dimensional equivalent resistance $\tilde{R}_{harv}$, as an independent figure of merit for evaluating the energy harvesting capability of different interface circuit, i.e.,

$$\tilde{R}_h = \frac{\max[E_{h,net}]}{\pi C_p V_{oc}^2}. \tag{6}$$

The energy harvesting capabilities of the series and parallel versions of SSHI can be obtained as follows

$$\tilde{R}_{h,\text{S-SMBF}} = \frac{M}{\pi}\frac{1-\gamma}{1+\gamma}; \tag{7}$$

$$\tilde{R}_{h,\text{P-SMBF}} = \frac{M}{\pi}\frac{1-\gamma}{1+\gamma} + \frac{1}{\pi}. \tag{8}$$

It can be observed from (7) and (8) that the harvesting capability increases with larger M, in other words, more bias-flip actions in each synchronized instant. For example, when $\gamma = -0.6$ (same parameters are used in the latter experiments), the energy harvesting capabilities of P-S7BF, P-S3BF, P-S1BF (parallel SSHI), and P-S0BF (SEH) have the ratios of 29 : 13 : 5 : 1.

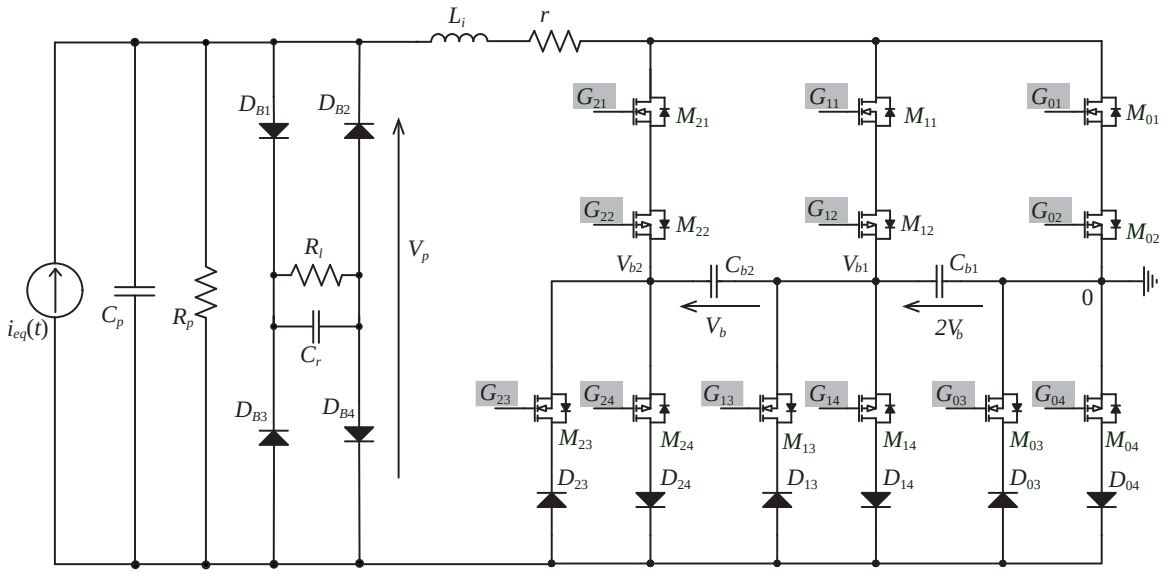


Fig. 3. P-S7BF circuit implementation.

TABLE I
SWITCHING SEQUENCE IN P-S7BF.

Bias-flip action	Conducting MOSFET	Bias voltage
Downstairs #1	M_{21}, M_{22}, M_{04}	$3V_b + V_d$
Downstairs #2	M_{11}, M_{12}, M_{04}	$2V_b + V_d$
Downstairs #3	M_{21}, M_{22}, M_{14}	$V_b + V_d$
Downstairs #4	M_{01}, M_{02}, M_{04}	V_d
Downstairs #5	M_{11}, M_{12}, M_{24}	$-V_b + V_d$
Downstairs #6	M_{01}, M_{02}, M_{14}	$-2V_b + V_d$
Downstairs #7	M_{01}, M_{02}, M_{24}	$-3V_b + V_d$
Upstairs #1	M_{01}, M_{02}, M_{23}	$-3V_b - V_d$
Upstairs #2	M_{01}, M_{02}, M_{13}	$-2V_b - V_d$
Upstairs #3	M_{11}, M_{12}, M_{23}	$-V_b - V_d$
Upstairs #4	M_{01}, M_{02}, M_{03}	$-V_d$
Upstairs #5	M_{21}, M_{22}, M_{13}	$V_b - V_d$
Upstairs #6	M_{11}, M_{12}, M_{03}	$2V_b - V_d$
Upstairs #7	M_{21}, M_{22}, M_{03}	$3V_b - V_d$

III. P-S7BF IMPLEMENTATION

A. Topology

The SMBF theoretical generalization has revealed a new prospect for future circuit improvement. Based on the prediction, Zhao and Liang have implemented the parallel synchronized triple bias-flip (P-S3BF) circuit towards higher harvesting capability in practice [10]. The current steering network, which is built with an auxiliary capacitor and several switch transistors and diodes, is the crucial part of the solution. In this paper, we reform the current steering network to make it more extensible towards the realization of more bias-flip actions. Moreover, the new current steering network design also helps realize a full use of the auxiliary capacitors towards more compact SMBF implementations.

The topology of P-S7BF implementation is shown in Fig. 3. A weakly coupled piezoelectric structure is modeled as the parallel combination of three parts: the equivalent current source $i_{eq}(t)$, which is proportional to the vibration velocity; the piezoelectric clamped capacitance C_p; and the shunt leakage resistance R_p. The bridge rectifier, which is composed of D_{B1} to D_{B4}, the filter capacitor C_r, and the dc load R_l, form the harvesting branch. The inductor L_i, its ESR r, and the current steering network form the bias-flip branch.

The current steering network is composed of three identical switch units. In each unit, the upper two cascading MOSFETs M_{x1} (NMOS) and M_{x2} (PMOS) ($x = 0, 1, 2$) actively enable or disable the bi-directional current flow. The lower part has two paths. One composed of M_{x3} (NMOS) and D_{x3} allows only the current flow in the upward direction. The other composed of M_{x4} (PMOS) and D_{x4} allows only the downward flow. The middle points of the three switch branches are connected by two auxiliary capacitors C_{b1} and C_{b2}. By properly controlling the switching sequence at each synchronized instant, a sophisticated charge flow can be produced through C_p towards larger net harvested power.

B. Switches Operation

The switching sequence is designed according to the optimal bias-flip (OBF) strategy, which was developed based on the SMBF generalization [11]. The OBF strategy of P-SMBF has two features: 1) The optimal bias voltages are symmetrically distributed about zero volt. 2) The voltage change of each bias flip is the same. Therefore, if we want to realize seven step bias flips, there should be seven bias voltages $3V_b$, $2V_b$, V_b, 0, $-V_b$, $-2V_b$, $-3V_b$, where V_b is a variable depending on the vibration level. As the bias voltage in P-S3BF is self-adaptive, in P-S7BF, we also assume that steady state can be automatically attained by proper switching sequence.

In practice, the volume of the auxiliary capacitor is much larger than transistors and diodes; therefore, the number of auxiliary capacitors should be minimized. The aforementioned seven bias voltages can be realized by fully using two bias

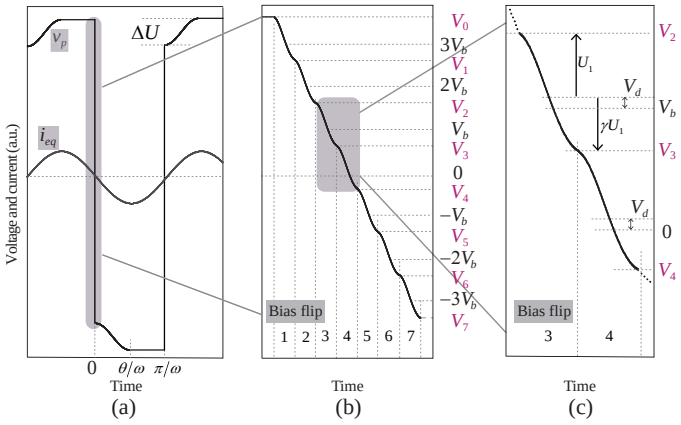


Fig. 4. Waveforms in P-S7BF. (a) Voltage and current overviews. (b) Enlarged view in the downstairs instant. (c) Enlarged view of the 3rd and 4th bias-flip actions.

sources and their combinations. In other words, two auxiliary capacitors can make up to seven bias-flip actions towards P-S7BF. The two capacitors in our design are C_{b1} and C_{b2}, as shown in Fig. 3. By conducting the switches according to Table I, when arriving at the steady state, the proportional relations, $V_{b1} = 2V_b$ and $V_{b2} = 3V_b$, will be automatically established. In the former three bias-flip actions, the charge from C_p flows through the series combination of C_{b1} and C_{b2}, C_{b1}, and C_{b2}, respectively. In the 4th action, v_p flips with respect to zero volt without crossing C_{b1} or C_{b2}. In the last three actions, the charge from C_{b2}, C_{b1}, and the series combination of C_{b1} and C_{b2} is injected back to C_p for pre-biasing v_p. Based on the definitions of two types of bias-flip actions [11], the former fours are passive bias-flip actions, while the latter three are active ones.

The voltage and current waveforms in P-S7BF are shown in Fig. 4. They are the embodiment of P-SMBF, where the number of bias-flip actions $M = 7$ [11]. By taking the forward voltage drop of the current steering diode V_d into consideration, the actual bias voltages are listed in the third column of Table I.

C. Steady-State Analysis

For better understanding the working principle of P-S7BF, some formulas are developed to describe the voltage changes. In steady state, the auxiliary capacitors are energy neutral in each vibration cycle, i.e., the energy absorbed from C_p equals to the energy pumped back to C_p later. All net harvested energy goes into the parallel branch which is composed of the bridge rectifier, filter capacitor C_r, and dc load R_l.

Given a harmonic excitation, which induces the equivalent sinusoidal current

$$i_{eq}(t) = I_0 \sin(\omega t), \tag{9}$$

where ω is the vibration frequency, I_0 is the current magnitude, the voltage across the piezoelectric element can be described with the piecewise equation as follows

$$v_p(t) = \begin{cases} -V_{oc}\cos(\omega t) + V_{oc} - V_7, & 0 \le \omega t < \theta; \\ V_0, & \theta \le \omega t < \pi; \\ -V_{oc}\cos(\omega t) - V_{oc} + V_7, & \pi \le \omega t < \pi + \theta; \\ -V_0, & \pi + \theta \le \omega t < 2\pi, \end{cases} \tag{10}$$

where $V_{oc} = I_0/(\omega C_p)$ is the nominal open-circuit voltage. θ is the blocked angle of the rectifier in a half cycle, which can be expressed as follows

$$\cos\theta = 1 - \frac{V_0 + V_7}{V_{oc}} = 1 - \frac{\Delta U}{V_{oc}}. \tag{11}$$

ΔU is the voltage difference between V_0 and $-V_7$, as shown in Fig. 4(a).

Given the voltage relationship illustrated in Fig. 4(b) and the bias voltages listed in Table I, the relations of intermediate voltages and bias voltages are formulated as follows

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ \gamma & -1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & \gamma & -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \gamma & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \gamma & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \gamma & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \gamma & -1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \gamma & -1 \end{bmatrix} \begin{bmatrix} V_0 \\ V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \\ V_6 \\ V_7 \end{bmatrix} = \begin{bmatrix} \Delta U \\ (\gamma-1)(V_{b2}+V_d) \\ (\gamma-1)(V_{b1}+V_d) \\ (\gamma-1)(V_{b2}-V_{b1}+V_d) \\ (\gamma-1)V_d \\ (\gamma-1)(-V_{b2}+V_{b1}+V_d) \\ (\gamma-1)(-V_{b1}+V_d) \\ (\gamma-1)(-V_{b2}+V_d) \end{bmatrix}. \tag{12}$$

Three additional equations can be obtained, given the energy neutral relations in C_{b1} and C_{b2}, i.e.,

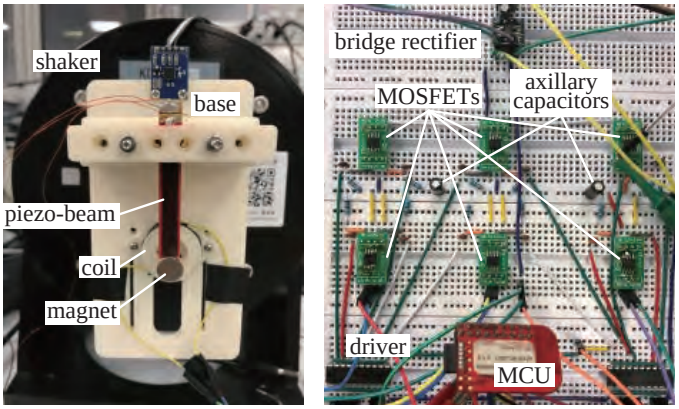
$$\begin{cases} V_0 - V_1 = V_6 - V_7 \\ V_1 - V_2 = V_5 - V_6 \\ V_2 - V_3 = V_4 - V_5 \end{cases}. \tag{13}$$

Substituting (13) into (12). The intermediate voltages in a downstairs bias-flip action are solved as follows:

$$\begin{bmatrix} V_0 \\ V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \\ V_6 \\ V_7 \end{bmatrix} = \frac{1}{1+\gamma} \begin{bmatrix} 7(\gamma-1)V_d + (4-3\gamma)\Delta U \\ 5(\gamma-1)V_d + (3-2\gamma)\Delta U \\ 3(\gamma-1)V_d + (2-\gamma)\Delta U \\ (\gamma-1)V_d + \Delta U \\ (1-\gamma)V_d + \gamma\Delta U \\ 3(1-\gamma)V_d + (2\gamma-1)\Delta U \\ 5(1-\gamma)V_d + (3\gamma-2)\Delta U \\ 7(1-\gamma)V_d + (4\gamma-3)\Delta U \end{bmatrix} \tag{14}$$

The seven voltage steps are evenly distributed between V_0 and V_7 making

$$U_1 = U_2 = \cdots = U_7 = \frac{\Delta U - 2V_d}{1+\gamma}, \tag{15}$$



(a) (b)

Fig. 5. Experimental setup. (a) Mechanical structure. (b) P-S7BF circuit.

TABLE II
CIRCUIT SPECIFICATIONS.

Parameter	Value
C_p	69.31 nF
f_0	52 Hz
L_i	1 mH
C_{b1},C_{b2}	4.7 μF
C_r	10 μF
γ	-0.6
Diode	SS16 ($V_d = 0.5$ V @ 100 mA)
MOSFET	Vishay Si4590DY
Bridge rectifier	MB6S

which agrees with the OBF strategy [11]. The bias voltage V_b in steady state can be obtained as follows

$$V_b = V_{b2} - V_{b1} = \frac{1-\gamma}{1+\gamma}(\Delta U - 2V_d). \tag{16}$$

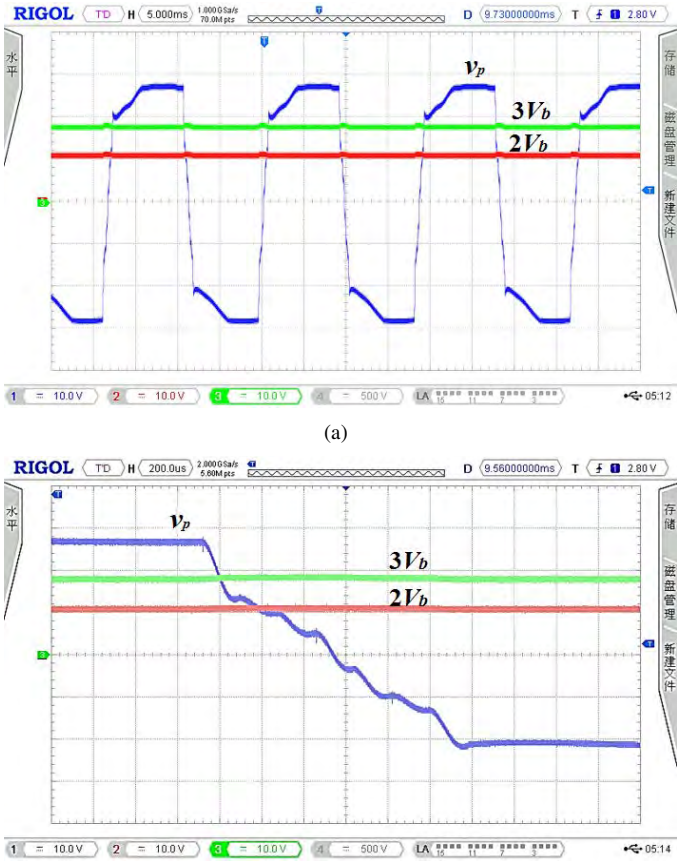
D. Transient

In the existing series synchronized double bias-flip (S-S2BF) technologies [7]–[9], additional controllable voltage sources are required for realizing the bias voltages. On the country, the proposed P-S7BF solution, like its P-S3BF brother [11], is self-contained and self-adaptive. These two significant features facilitate the stand-alone implementation of P-S7BF towards practical applications. The self-adaptive feature is guaranteed because there is a steady-state solution of V_b in P-S7BF, which was proved and shown in (16). The transient analysis of P-S7BF will be similar to, but more complicated than that of P-S3BF. Both circuit simulation and experiment show that the voltages across C_{b1} and C_{b2} can always maintain a ratio of 2 : 1 at steady state by repeating the switching sequence listed in Table I. The detailed transient operation towards the steady-state operation will be investigated in our future work.

IV. EXPERIMENT

A. Setup

Experiments are carried out to validate the P-S7BF circuit design. The experimental setup is shown in Fig. 5(a).



(a)

(b)

Fig. 6. Experimental voltage waveforms. (a) The overview of v_p. (b) The enlarged view at a downstairs instant.

The piezoelectric cantilevered structure is subject to a base vibration, which is provided by a shaker. An accelerometer is installed at the moving base for sensing the acceleration and stabilizing the excitation conditions. The whole electromechanical system vibrates at its first vibration mode. A velocity sensor, which is composed of a coil and a permanent magnet, is installed at the free end of the cantilever for sensing the beam deflection. Once the synchronized current-zero-crossing instant is attained, a micro-controller carried out the seven bias-flip actions in succession.

The experimental P-S7BF circuit is currently built on a breadboard, whose picture is shown in Fig. 5(b). The driver circuits for the PMOS and NMOS devices are similar to those used in the former P-S3BF implementation [10]. The detailed circuit specifications are listed in Table II.

B. Result

Fig. 6(a) shows the experimental waveforms of v_p. The enlarged view at a downstairs synchronized instant is shown in Fig. 6(b). Seven bias-flip actions are successfully realized under the steady-state operation. From the voltage profile shown in Fig. 6(a), making more bias-flip actions has the same effect as making an SSHI with smaller γ (corresponding to larger Q factor), which implies higher extracted power. On

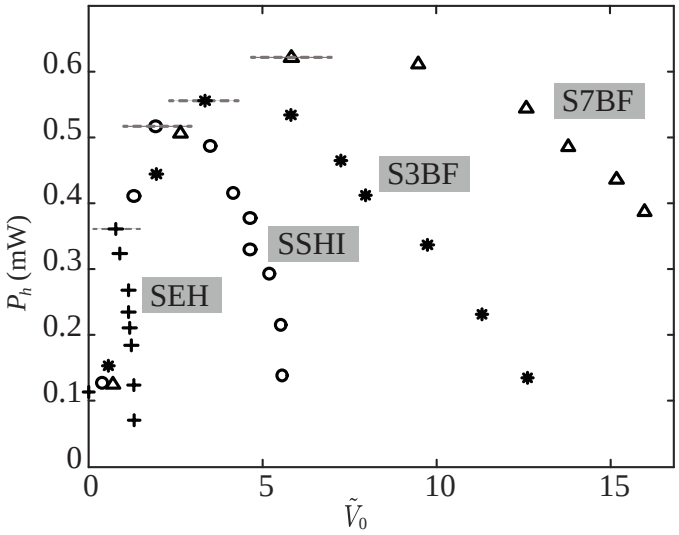


Fig. 7. Experimental results on harvested power.

the other hand, for making the same v_p profile, the switch dissipation by using the multiple bias-flip actions is much lower than that by using a single-bias-flip SSHI. Therefore, the net harvested power, as the difference between extracted and dissipated powers, increases by taking multiple bias-flip solutions.

Some insufficiencies, which should be subject to future improvement, are observed from the v_p waveform in Fig. 6(b). For example, the first and seventh voltage steps are larger than other steps. The unevenly distributed steps will be better alleviated by using a more reliable printed circuit board (PCB) version in the future.

The energy harvesting capability (proportional to the maximum harvested power) of P-S7BF is comparatively studied with that of other popular or recent solutions, including SEH, P-SSHI, and P-S3BF, in experiment. Fig. 7 shows the harvested power in these solutions, as functions of the normalized rectified voltage $\tilde{V}_0$. In experiment, $\tilde{V}_0$ is tuned and stabilized by connecting different dc load resistor R_l in the circuit. The experimental results demonstrate that, under the same base excitation, the P-S7BF interface circuit outperforms SEH, P-SSHI, and P-S3BF, in terms of harvested power. The ratios of their harvested power (P-S7BF : P-S3BF : P-SSHI : SEH) are 1.75 : 1.56 : 1.45 : 1.

The ratios of harvested power here are different from those predicted by (8). It is worth to note that, the energy harvesting capability of an interface circuit is not the only determinant of harvested power. Both the dielectric loss [12] and the increase of electrically induced damping [13] might counteract the harvested power enhancement in a dynamic PEH system. The joint electromechanical effect will be investigated in our future work.

V. Conclusion

This paper has introduced the design and implementation of the parallel synchronized septuple bias-flip (P-S7BF) circuit for piezoelectric energy harvesting (PEH) enhancement. As a new instance developed based on the synchronized multiple bias-flip (SMBF) model, the steady-state operation of P-S7BF is analyzed in detail. Experimental results under base excitation validated that P-S7BF outperforms the existing and representative circuit solutions, including the recently proposed P-S3BF. Therefore, by making the full use of two auxiliary capacitors, the well-targeted and innovative P-S7BF circuit has refreshed the record of the most capable PEH interface circuit.

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