A Self-Powered Piezoelectric Energy Harvesting Interface Circuit Based on Adaptive SSHI With Fully Integrated Switch Control

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***Abstract*—This paper presents a piezoelectric energy harvesting (PEH) interface circuit, which integrates an adaptive synchronized switch harvesting on inductor (SSHI) circuit and an active rectifier. The proposed adaptive SSHI circuit utilizes the signal of the active rectifier to control the synchronized switch so that the external control is not needed and the proposed PEH circuit can be effective for varies inductance. The active rectifier circuit and the switch control circuit of this paper are directly powered by the storage capacitor, which avoids the auxiliary power supply. As a result, the PEH interface circuit is self-powered. The proposed circuit has been designed in 0.18-μm CMOS technology, and the simulated power consumption of the control part is 0.178 μ W. The simulation result shows the output power is 4.6 times of that in the ideal full-bridge rectifier. Moreover, without any external power supply, it is capable of cold startup to provide a stable output voltage.**

Keywords—Piezoelectric energy harvesting, adaptive SSHI, active rectifier, self-powered, cold startup

I. INTRODUCTION

Energy harvesting can collect energy from ambient environment and continuously convert it into usable electrical energy as a stable power supply. Therefore, it can be used widely in the applications such as wireless sensor network (WSN) node, etc. For example, many piezoelectric energy harvesting (PEH) circuits have been proposed to convert the vibration energy to DC power supply [1−12].

According to the equivalent electrical model of the piezoelectric sensor [1−3], in the process of energy collection, the charge and discharge of the internal capacitance will cause energy loss, which seriously affects the efficiency of energy collection. Meanwhile, as the output power of the harvester is often very low, the PEH circuit should feature with low power consumption and high-power efficiency. The traditional implementation for PEH is to use a fully-bridge (FB) rectifier. However, the charge on the internal capacitor cannot be utilized and the turn-on voltage drop is often large. As a result, the power conversion efficiency, or the output power, is often very low. A synchronized switch harvesting on inductor (SSHI) circuit has been proposed to reduce the charge loss on the capacitor, by flipping the internal capacitor voltage in a very short time through the *LC* resonant circuit [5]. One of the key issues in SSHI circuit is how to achieve accurate flipping time control for different resonant frequency, i.e., different capacitance in harvester or different inductance in SSHI circuit. Manually configuring were realized through an external 8-bit digital control circuit [6] or an external variable resistor [8]. In order to achieve automatically adaptive control, a passive diode was inserted on each resonant loop in a PCB-level circuit to adaptively setting the flipping time [7], which has been further improved and implemented in an integrated circuit with active rectifiers and cold-startup capability [9]. However, the circuit performance on different inductance has not been well demonstrated, and the control is complicated which degraded the power efficiency and may introduce timing error.

In this paper, a self-powered piezoelectric energy harvesting interface circuit based on adaptive SSHI circuit and active rectifier is proposed. The hysteresis comparator is adopted to detect the voltage across of the diode on each resonant loop. Based on the output signals of the comparator in the active rectifier and the hysteresis comparator, the voltage across the capacitor is flipped adaptively at the optimum time without the need to configuring the switching time. In that case, a precisely adaptive SSHI with simple control circuit thus low power consumption is achieved. Moreover, the whole circuit is powered by the charge on the storage capacitor, so that the self-powered rectification and cold start are realized.

The basic principles and the circuit implementation are introduced in Section II. The simulation results and relevant discussions are presented in Section III. Finally, Section IV summarizes the paper.

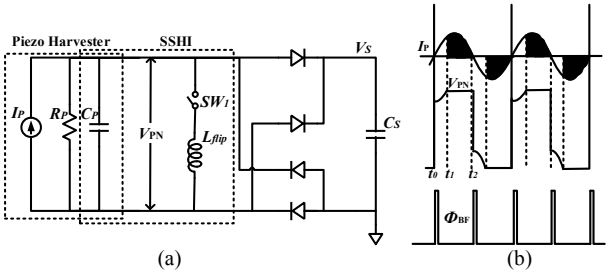

Fig. 1. SSHI circuit for PEH and the associated waveforms, (a) structure diagram of SSHI circuit, and (b) working waveforms.

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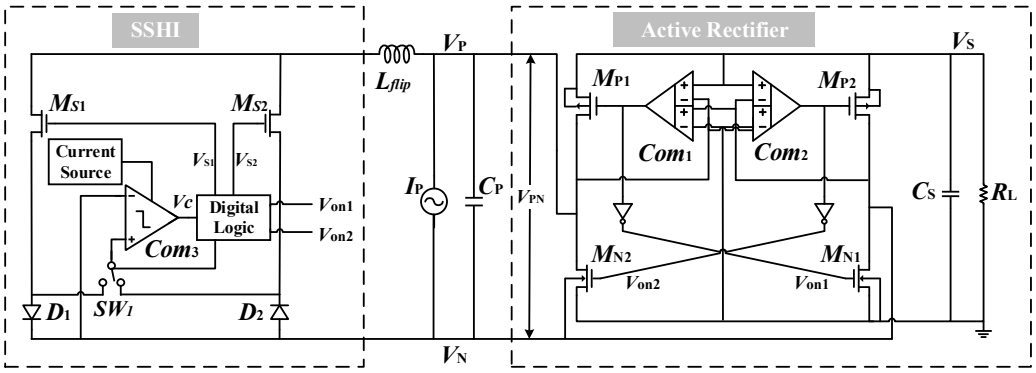

Fig. 2. Simplified diagram of the proposed self-powered SSHI interface circuit.

II. Implementation of the Proposed Adaptive SSHI

The basic principle of the SSHI circuit is to flip the charge on the internal capacitor through *LC* resonant [5]. As shown in Fig. 1, when the input current I_P passes through the zero point, the switch SW_1 is closed, and the inductor flips the voltage across the capacitor C_P until the current flowing through the inductor is zero. When the flipping process is ended, the switch SW_1 is disconnected and then the rectifying process starts again.

The proposed PEH interface circuit is shown in Fig. 2. It consists of an adaptive SSHI circuit and an active rectifier. The SSHI circuit includes a rail-to-rail hysteresis comparator, a switching control circuit and a current source circuit. The active rectifier includes four active diodes ($M_{N1,2}$; $M_{P1,2}$), pair of which consists of two self-biasing comparators [10] and four switching transistors. The power to all active circuit is supplied by the charge on capacitor C_S.

In addition to the self-powered feature, the proposed SSHI interface circuit uses the output voltage of the comparator in the active rectifier circuit as the trigger signals to start the SSHI [11], [12]. In order to fine control the end of the voltage flipping process, a rail-to-rail hysteresis comparator is used to monitor the voltage across the diode. Moreover, the hysteresis comparator is based on time division multiplexing, which can reduce the static power consumption of the circuit.

The working principle of the proposed self-powered SSHI interface circuit is as follows. When the voltage across C_P is charged to be higher than V_S, the self-biased comparator Com_1 outputs a low-level signal, causing the switching transistor M_{P1} to turn on, and the switching transistor M_{N1} is turned on too, thereby forming a clockwise rectifying conduction loop. The active rectifier circuit starts to work and the current source I_P charges the storage capacitor C_S. When the current I_P passes through the zero point, the charging process is ended. At the same time, the single-pole double-throw switch SW_1 is connected to diode D_1, and the switching transistor M_{S1} is turned on. As a result, the internal capacitor C_P, the inductor L, the switch M_{S1} and the diode D_1 form an *LC* resonant circuit. The hysteresis comparator Com_3 controls the digital logic module to output a low-level signal at the end of half of the *LC* resonant period by detecting the voltage difference across the diode D_1, so that the switch M_{S1} is turned off, thereby effectively flipping the voltage across C_P. Conversely, the working process of the current source I_P in the negative half cycle is similar.

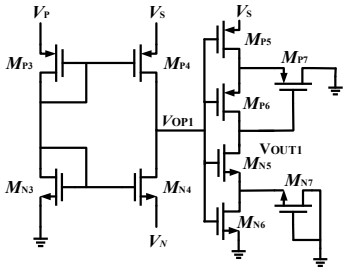

Fig. 3. The proposed self-biased common-gate comparator with unbalanced Schmitt trigger.

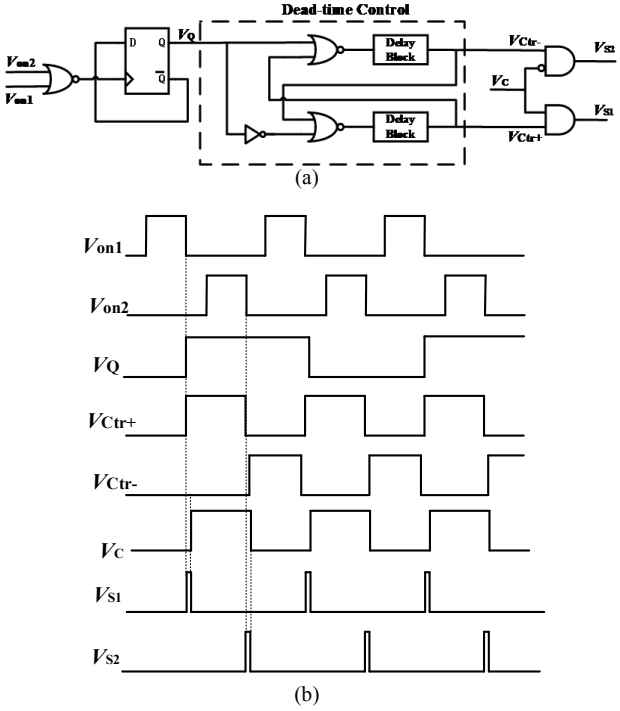

Fig. 4. (a) Switching signal control circuit for SSHI and (b) the associated working phases.

A. Comparator Circuit in Active Rectifier

The proposed self-biased common-gate comparator with unbalanced Schmitt trigger in the active rectifier is presented in Fig. 3, which is the comparator Com_1 in Fig. 2. Compared to the traditional common-source comparator, the self-biased common-gate comparator has a wider input voltage range and does not require additional current source for biasing [10]. Due to this merit, it is very suitable to be the comparator in the

active diode circuit. For the comparator Com_1 in Fig. 3, the voltages V_P across the C_P and V_S across the C_S are the input signals of the self-biased comparator Com_1.And the V_{OP1} is the output signal. When the voltage V_P is less than the voltage V_S, M_{P4} turns on and M_{P4} is in the off state. The comparator Com_1 outputs a high-level signal V_{OP}. When the voltage V_P is more than the voltage V_S, it is reversed. But when the output of the comparator rises from low voltage to high voltage, it is often accompanied by a voltage glitch in the output of the other comparator, i.e., Com_2 in this paper. This glitch may wrongly trigger the following inverter. Therefore, the Schmitt triggers is adopted in this paper to eliminate this effect. Since the glitch only exists when each comparator output rises from low voltage to high voltage, the gate of M_{N7} is grounded and M_{N7} is always in the off state. In that case, the power consumption can be reduced.

B. Switching Signal Control for SSHI

The circuit diagram of the switch control for SSHI and the associated working phases are shown in Fig. 4. As can be seen from the Fig. 4(a), the circuit mainly includes a dead-time control module and a combination logic module. The signals V_{ON1} and V_{ON2} are the output of the comparators in the active rectifier. After an OR operation, they are inputted in the D flip-flop as clock signal. The output of the D flip-flop passes through the dead-time control module. The falling edge of the D flip-flop takes precedence, and two high-level non-overlapping signals V_{Ctr+} and V_{Ctr-} are generated. Finally, after an AND operation with the output signal of the hysteresis comparators, i.e., V_C, V_{Ctr+} and V_{Ctr-}, control signals for M_{S1} and M_{S2} (V_{S1} and V_{S2}) are generated respectively. The associated working phases are shown in Fig. 4(b). It is worth noting that the power supply in the switch control circuit is also provided by the storage capacitor.

III. Simulation Results and Discussions

The proposed PEH interface circuit has been designed in 0.18-μm CMOS technology. The simulated start-up procedure is shown in Fig. 5(a), where I_P is set to be a 50-Hz sinusoidal current signal with 20-μA amplitude, and C_P = 30 nF, Cs = 1 μF, L_{flip} =1 mH, and R_L = 1 MΩ. It can be found the start-up time is 2.5 s, and the steady DC output voltage is 4.78 V. Fig. 5(b) shows the zoom-in waveform of the voltage across the capacitor C_P, i.e., V_{PN}. During the process of flipping V_{PN} from positive to negative, V_{PN} is flipping from 4.78 V to −3.38 V, and the flipping efficiency is 70.71%. During the process of flipping V_{PN} from negative to positive, V_{PN} is flipping from −4.78 V to 2.88 V, and the flipping efficiency is 60.25%. It should be noted that in different conditions, the source voltages in switching NMOS transistors are different. In that case, the flipping efficiencies are different due to different on-resistances resulted by the body effect.

The power consumption of the proposed PEH interface circuit is also simulated based on the same condition. The simulated power consumption of the digital part of the switching control circuit is about 8.37 nW, and the power consumption of the hysteresis comparator and current source are around 178 nW. The comparator in the active diode is a self-biased comparator, the maximum current in the static state is about 2.91 μA. As a result, the main power consumption of the proposed PEH circuit is extremely low, and capable of cold start without external power.

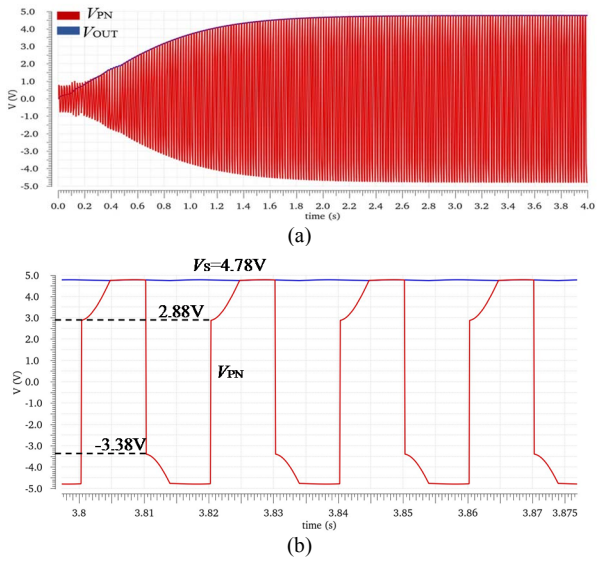

Fig. 5. Simulated (a) transient waveform and (b) the zoom-in waveform of (a).

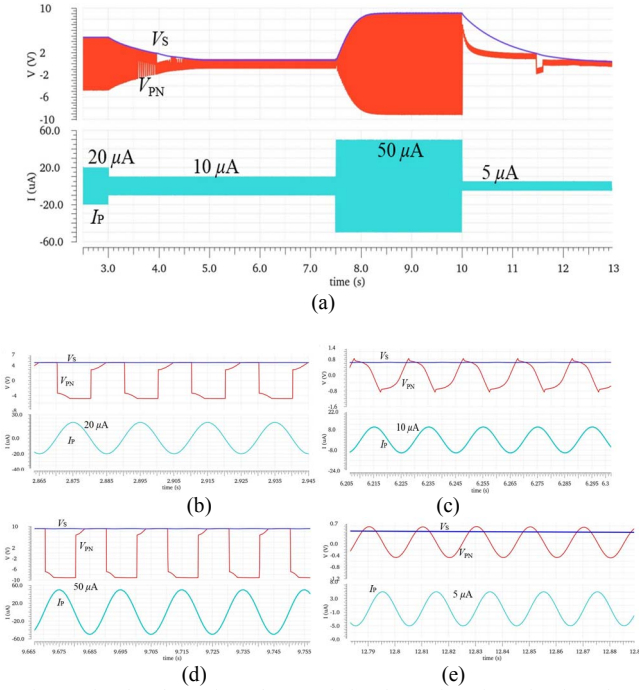

Fig. 6. Simulated transient characteristic of PEH interface circuit under different input currents, (a) transient characteristic under current variation, (b) 20-μA input current, (c) 10-μA input current, (d) 50-μA input current, and (e) 5-μA input current.

The simulated transient characteristics of the proposed PEH circuit with different input current are shown in Fig. 6. When I_P is reduced from 20 μA to 10 μA, V_{PN} is reduced, and the voltage flipping process fails, while the active rectifier still works normally. When I_P is increased from 10 μA to 50 μA, the SSHI circuit start rectifying process. It has also been proven that the proposed circuit has a cold-start capability convincingly. When I_P is reduced from 50 μA to 5 μA, V_{PN} becomes a sine wave because the bias-flip process fails, and the rectifying process is actually performed through the parasitic diode of the MOS transistors (MN2 and MP2).

The proposed PEH interface circuit is compatible with different harvester or flipping inductance due to the proposed

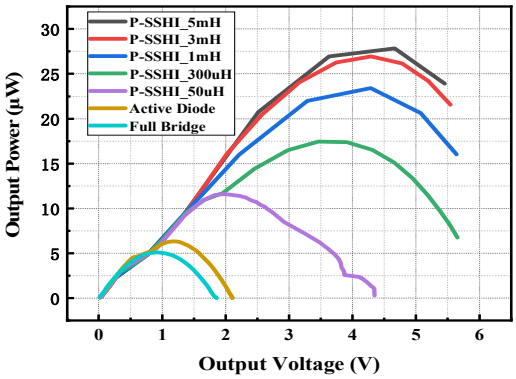

Fig. 7. Simulation of output power vs output voltage of SSHI and FB rectifier circuits

adaptive control for SSHI. The simulated output power versus output voltage of the proposed circuit and traditional FB rectifier are shown in Fig. 8. If the harvester is fixed, the flipping inductance can be varied from 50 μH to more than 5 mH. This is a very key point as it can be widely used in different applications. When the flipping inductance is 1 mH, the maximum output power is about 23.4 μW, which is 4.6 times of that in the FB rectifier. Moreover, as the flipping inductance increases, the maximum output power continues to increase.

The main performance comparison between proposed circuit and the state-of-the-art designs is shown in TABLE I. The proposed circuit not only has the capacity of fully integrated adaptive flipping control and self-powered cold start, but also has relatively high energy harvesting efficiency, which is improved by 4.6 times comparing with the traditional FB rectifier. Although the interface circuit in [7] can obtain highest energy acquisition efficiency among these designs, it cannot cold start without external power, and the static power consumption is not considered, which actually has a high impact on energy harvesting efficiency. The circuits proposed in [6] and [8] feature with self-powered cold-start capability, but for different piezoelectric harvesters and inductors, manually configure through an external digital control or variable resistor is needed to adapt the flipping time.

IV. Conclusion

This paper presents a self-powered and fully adaptive piezoelectric energy harvesting circuit in 0.18-μm CMOS technology. The proposed circuit can work well for different flipping inductance or piezoelectric harvesters with fully integrated control. An active rectifier with unbalanced Schmitt trigger to further reduce the static power consumption and thus increase power efficiency. In addition, the cold-start capability ensures that the circuit can work properly without external wake-up. Compared with the classical full-bridge rectifier circuit, the energy extraction efficiency is improved by 4.6 times in typical condition.

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TABLE I. Performance Comparisons with Recent PEH Interface Circuits

	[6] JSSC 2010	[7] TPEL 2015	[8] ISSCC 2016	[9] TCAS-I 2017	**This work** ISCAS 2020
Implementation	Integrated	Discrete	Integrated	Integrated	Integrated
C_P (nF)	18	18	9	19	30
f_P (Hz)	225	225	229	144	50
I_P (μA)	63	63	None	None	20
L (μH)	820	940	3300	220	50 ~ 5000
Flipping control	Manually, external	Adaptive, external	Manually, external	Adaptive, fully integrated	Adaptive, fully integrated
Self-power	Yes	No	Yes	Yes	Yes
FOM: P/P_{FB}	>4x	5.8x	4.4x*	2.1x*	4.6x

* Compared with the ideal full-bridge rectifier output power