Analog Integr Circ Sig Process (2011) 67:149–156
DOI 10.1007/s10470-010-9568-3

Analysis and design of Class-E power amplifiers at any duty ratio in frequency domain

Tianliang Yang · Junrui Liang · Chunyu Zhao · Dayue Chen

Received: 18 January 2009 / Revised: 14 October 2010 / Accepted: 20 November 2010 / Published online: 7 December 2010
© Springer Science+Business Media, LLC 2010

Abstract This paper presents a design method for Class-E power amplifiers based on the analysis of the load impedance in the frequency domain. The analytical expressions of the design parameters are derived as functions of the duty ratio D and angular frequency ω_0 of the gate driven voltage of the switch. According to the analysis, for an optimal Class-E amplifier that meets both the zero-voltage switching (ZVS) and the zero-derivative switching (ZDS) conditions, the increase of the duty ratio D results in the decrease of the DC input resistance, and this consequently increases the input power and decreases the total efficiency. Two design procedures for different design purposes are discussed under three cases with different duty ratios, i.e. $D = 0.25$, 0.5 and 0.75. The simulation and experimental results of these cases agree well with the theoretical ones.

Keywords Class-E power amplifier · Zero-voltage switching (ZVS) · Zero-derivative switching (ZDS)

1 Introduction

The Class-E power amplifier introduced by N.O. Sokal and A.D. Sokal [1] is widely used in the applications of DC–AC, DC–DC power conversion [2] and RF field [3] due to its high efficiency and simple circuit topologies. However, it is a difficult task to calculate the accurate parameters of a Class-E power amplifier through solving the a binary quadratic differential governing equations directly, that some reasonable assumptions, i.e. high value of the load quality factor Q and large value of the choke coil, are normally included in the design analysis. Under these assumptions, a number of design methods of the Class-E amplifier have been developed [4–6]. Kazimierczuk and Puczko [5] presented their design tables on some circuit parameters as functions of Q by Laplace-transform and numerical solution. N.O. Sokal [6] proposed a numerical table, which is similar to that in [5], and concluded some fitted expressions of each component with respect to Q. It is applicable to design a Class-E amplifier according to the tables provided in [5, 6]. However, these tables cannot intuitively explain the characteristics of the Class-E amplifier, e.g. the phase difference between the output voltage and the driving square wave. Suetsugu [7] used the single parameter of ϕ (the initial phase of the load current) to analyze the off-nominal Class-E at 50% duty ratio, and extented his work by analyzing a design case at any duty ratio [8]. Their researches indicate that the main circuit parameters are determined by ϕ, not by Q.

In this paper we present a frequency-domain method for the analysis and design of the Class-E amplifier at any duty ratio. In this method, with the same preliminary assumptions as [5], the steady-state current and voltage waveforms of the Class-E amplifier can be determined by the zero-voltage switching (ZVS) and zero-derivative switching (ZDS) conditions. By analyzing the steady-state switch voltage and output current, the load impedance Z is expressed as a function of the duty ratio D and angular frequency ω_0 of the gate voltage. In addition, the DC input resistance, the minimum loaded quality and the power loss on the switch-on resistance can be expressed as functions of D. Based on these analyses, two design procedures

T. Yang · J. Liang · C. Zhao · D. Chen (✉)
Department of Instrument Science and Engineering, School of Electronics, Information and Electrical Engineering, Shanghai Jiao Tong University, Shanghai 200240, People's Republic of China
e-mail: dychen@sjtu.edu.cn

for different purposes with $D = 0.25$, 0.5 and 0.75 are presented.

2 Voltage and current waveforms

The circuit topology of a basic Class-E amplifier is shown in Fig. 1, with the following assumptions [5, 7].

(1) The choke inductor L_{RFC} is lossless and its inductance is large enough to neglect its ripple current.
(2) The MOSFET is an ideal switch component (turning on and off instantly), so that it has zero on-resistance and infinite off-resistance.
(3) The loaded quality factor Q of the output resonant network is high enough so that the output current can be regarded as a pure sinusoid.

If the sinusoidal output current i_o and the gate voltage v_g in the circuit are determined, under the required conditions of ZVS and ZDS, the waveforms of the current and voltage at any point may be obtained with the following analyses.

According to the Assumption 3, the steady-state output current i_o is a sinusoid, as shown in Fig. 2(a), which can be described as

$$i_o(\theta) = I_m \sin\theta \tag{1}$$

where I_m is the current amplitude and $\theta = \omega_0 t$ is the phase angle with the angular frequency ω_0. The analyses of the circuit are confined in any one cycle k of $i_o(\theta)$, $\theta \in [(2\,k-1)\pi, (2\,k+1)\pi)$.

Considering the ZVS condition, at the switch-off duration, the shunt capacitance C should be charged and then discharged to achieve $i_C = 0$ as well as $v_C = 0$ when the switch turns on. In addition, to satisfy the ZDS condition, the current through the switch, i_S, should be zero when the switch turns on. According to the Kirchhoff's current law, both $i_C = 0$ and $i_S = 0$ can and only can be achieved if the output current i_o equals to the supply current I_{DD}, i.e. $i_o = I_{DD}$, (see Fig. 1). This condition can be satisfied at two phase angles θ_k' (where i_o slopes up to cross I_{DD}) and θ_k'' (where i_o slopes down to cross I_{DD}), as shown in Fig. 2(a). Since the shunt capacitance charges ($i_o < I_{DD}$) then discharges ($i_o > I_{DD}$) in a switch-off duration, the switch must turn on at θ_k'' due to $i_o > I_{DD}$ ahead of this turn-on point.

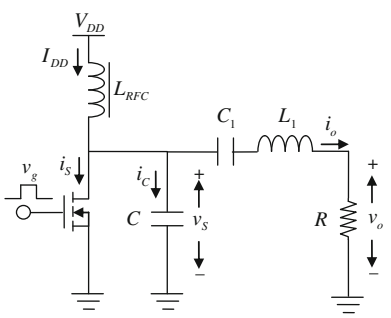

Fig. 1 Basic circuit of the Class-E amplifier

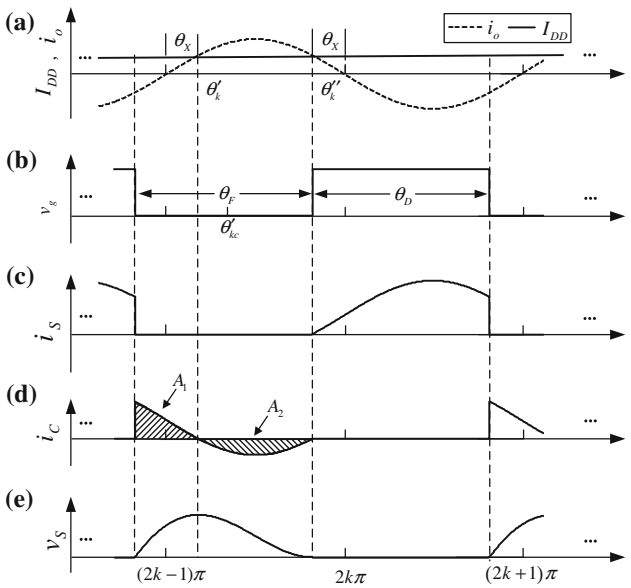

Fig. 2 Steady-state voltages and currents of an ideal Class-E amplifier. **a** Input and output current. **b** Gate voltage across the switch. **c** Current through the switch. **d** Current through the shunt capacitance. **e** Drain voltage across the switch

The angle phase difference between θ_k' and $(2\,k-1)\pi$ is defined as

$$\theta_X = \theta_k' - 2(k-1)\pi. \tag{2}$$

From (2), the supply current I_{DD} equaling to i_o at θ_k' can be expressed as

$$I_{DD} = I_m \sin(\theta_k') = I_m \sin(\theta_X). \tag{3}$$

The gate driven voltage v_g, as shown in Fig. 2(b), is a periodic square wave with the duty ratio of D. Therefore, the phase duration of the switch-on is

$$\theta_D = 2\pi D \tag{4}$$

and the phase duration of the switch-off is

$$\theta_F = 2\pi(1-D). \tag{5}$$

The center radian in the switch-off duration θ_{kc}' can be expressed as

$$\theta_{kc}' = (2k-1)\pi - \theta_X + \frac{\theta_D}{2}. \tag{6}$$

When the switch is on, the current through it (see Fig. 2(c)) can be expressed as

$$i_S(\theta) = [I_{DD} - I_m \sin(\theta)]s(\theta) \tag{7}$$

where $s(\theta) = \begin{cases} 1 & \theta_k'' < \theta \le \theta_k'' + \theta_D \\ 0 & \theta_k'' - \theta_F < \theta \le \theta_k'' \end{cases}$.

When the switch is off, the current through the shunt capacitance, as shown in Fig. 2(d), can be expressed as

$$i_C(\theta) = (I_{DD} - I_m \sin\theta)[1 - s(\theta)]. \tag{8}$$

According to the ZVS condition, in the switch-off duration, the input charge to the shunt capacitance C, which is proportional to the area of A_1, and the discharged charge, which is proportional to the area of A_2, are equal, i.e., $A_1 = A_2$, which can determine the relationship between θ_X and θ_D as follows.

As shown in Fig. 2(d), A_1 is the area under i_C (given in (8)) over the duration $[\theta''_{k-1} + \theta_D, \theta'_k]$:

$$\begin{aligned} A_1 &= \int_{\theta''_{k-1}+\theta_D}^{\theta'_k} |I_{DD} - I_m \sin\theta| d\theta \\ &= I_{DD}(\pi - 2\theta_X + \theta_D) + I_m[\cos\theta_X + \cos(\theta_X - \theta_D)] \end{aligned} \tag{9}$$

and A_2 is the area above i_C over the duration $[\theta'_k, \theta''_k]$

$$A_2 = \int_{\theta'_k}^{\theta''_k} |I_{DD} - I_m \sin\theta| d\theta = 2I_m \cos\theta_X - I_{DD}(\pi - 2\theta_X). \tag{10}$$

Thus, comparing (9) and (10) with their equivalent relationship, the difference on the angle phase θ_X can be expressed as a function of the angle phase of switch on θ_D:

$$\theta_X = \tan^{-1}\frac{1 - \cos\theta_D}{2\pi - \theta_D + \sin\theta_D}. \tag{11}$$

According to (11), the relationship between the ratio of $I_{DD}/I_m = \sin\theta_X$ (from (3)) and the switch duty ratio $D = \theta_D/2\pi$ (from (4)) can be obtained and shown in Fig. 3. From Fig. 3, as D increases, it is obvious that I_{DD}/I_m increases. This results in the decrease of the output current amplitude I_m for a constant supply current I_{DD}.

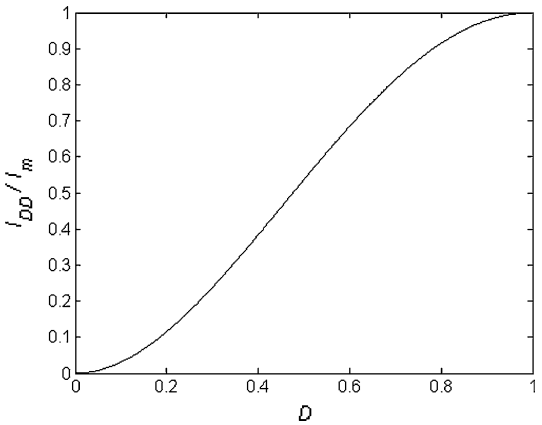

Fig. 3 Ratio of I_{DD}/I_m with respect to the duty ratio D

Consequently, due to the decrease of I_m, the load resistance R increases to sustain the relationship that the output power equals the input power.

During the switch on, the drain voltage of the switch v_S keeps zero, while, during the switch off, it increases from zero in the charge process ($\theta''_{k-1} + \theta_D < \theta \le \theta'_k$) and it falls to zero in the discharge process ($\theta'_k < \theta \le \theta''_k$), as shown in Fig. 2(e).

3 Circuit parameters

The load impedance Z, the DC input resistance R_{DC}, the minimum quality factor of the load branch $Q_{L\min}$, the input power P_{in}, the output power P_{out}, and the collect efficiency η_c are analyzed in terms of the switch-on interval θ_D as follows.

The load branch network consists of a resistance R, a capacitance C_1 and an inductance L_1. The impedance of the load branch network at the resonant frequency ω_0 can be expressed as

$$Z(\omega_0) = R + jX(\omega_0) \tag{12}$$

where $X(\omega_0) = \omega_0 L_1 - 1/\omega_0 C_1$.

$Z(\omega_0)$ can also be calculated from the frequency-domain relationship between the switch voltage v_C and the output current i_o, which is

$$Z(\omega_0) = \frac{V_C(\omega_0)}{I_o(\omega_0)} \tag{13}$$

where $V_C(\omega_0)$ and $I_o(\omega_0)$ are the Fourier coefficients of $v_C(t)$ and $i_o(t)$ at ω_0.

Considering the average of i_C in a cycle is zero, $V_S(j\omega)$ is

$$V_S(j\omega) = \frac{I_C(j\omega)}{j\omega C} \tag{14}$$

where the Fourier transfer function of i_C is

$$\begin{aligned} I_C(j\omega) = I_m \sum_{p=-\infty}^{\infty} \Bigg\{ &\sin\theta_X \frac{2\sin\frac{p\theta_F}{2}}{p} e^{-jp\theta''_{kc}} \\ &+ \frac{\sin\frac{(p-1)\theta_F}{2}}{p-1} e^{-j[(p-1)\theta'_{kc} - \frac{\pi}{2}]} + \frac{\sin\frac{(p+1)\theta_F}{2}}{p+1} e^{-j\left[(p+1)\theta'_{kc} + \frac{\pi}{2}\right]} \Bigg\} \\ &\delta(\omega - p\omega_0) \end{aligned} \tag{15}$$

where $\delta(\omega)$ is the Dirac delta function, and p is an integer.

From (14), let $\theta_c = \theta_D/2 - \theta_X$, the DC component of v_C is

$$V_S(0) = \frac{I_m}{2\pi\omega_0 C}\alpha \tag{16}$$

where

$$\alpha = -\theta_F\theta_c \sin\theta_X + 2\theta_c \sin\frac{\theta_D}{2}\sin\theta_c + \left(\theta_F \cos\frac{\theta_D}{2} + 2\sin\frac{\theta_D}{2}\right)\cos\theta_c. \quad (17)$$

And the Fourier coefficients of v_C at the fundamental frequencies ω_0 and $-\omega_0$ are

$$V_S(\omega_0) = \frac{I_m}{2\pi\omega_0 C}\left\{-j2\sin\theta_X \sin\frac{\theta_D}{2}e^{-j\theta_c} + \frac{\sin\theta_D}{2}e^{-j2\theta_c} + \frac{\theta_F}{2}\right\} \quad (18)$$

and

$$V_S(-\omega_0) = \frac{I_m}{2\pi\omega_0 C}\left\{j2\sin\theta_X \sin\frac{\theta_D}{2}e^{j\theta_c} + \frac{\sin\theta_D}{2}e^{j2\theta_c} + \frac{\theta_F}{2}\right\}. \quad (19)$$

Since the choke coil L_{RFC} is lossless (Assumption 1), the supply voltage V_{DD} is equal to the DC component $V_S(0)$ in (16), which is

$$V_{DD} = \frac{I_m}{2\pi\omega_0 C}\alpha. \quad (20)$$

And the voltage component at ω_0 can be expressed as

$$v_{SF}(t) = V_S(\omega_0)e^{j\omega_0 t} + V_S(-\omega_0)e^{-j\omega_0 t}. \quad (21)$$

The Fourier coefficient of the output current $i_o(t)$ (see (1)) is

$$I_o(\omega_0) = \frac{I_m}{2j}. \quad (22)$$

Substitution of (18) and (22) into (13) gives the load-branch impedance $Z(\omega_0)$ as

$$Z(\omega_0) = \frac{1}{2\pi\omega_0 C}\{\beta + j\gamma\} \quad (23)$$

where

$$\beta = [\sin\theta_X + \sin(\theta_D - \theta_X)]^2 \quad (24)$$

and

$$\gamma = \theta_F \cos 2\theta_X + \sin\theta_D \cos 2\theta_c. \quad (25)$$

Comparing the real and imaginary terms in (12) and (23) respectively, the circuit parameters in the load branch network can be determined:

$$R = \frac{1}{2\pi\omega_0 C}\beta \quad (26)$$

and

$$X(\omega_0) = \frac{1}{2\pi\omega_0 C}\gamma. \quad (27)$$

From (26) and (27), the non-dimensional design parameters $\omega_0 RC$ and $\omega_0 X(\omega_0)C$ as functions of the duty ratio D are calculated and shown in Fig. 4. The maximum value of $\omega_0 RC$ is 0.25 at $D = 0.35$. However, the Class-E amplifier cannot meet both ZVS and ZDS conditions if $\omega_0 RC$ is larger than 0.25. If $\omega_0 RC$ is between 0 and 0.25, there are two duty ratios will satisfy (26) and (27), so the Class-E amplifier can meet both ZVS and ZDS conditions at those two duty rations. However, the output power and components except R and C are not equal at these two duty ratios.

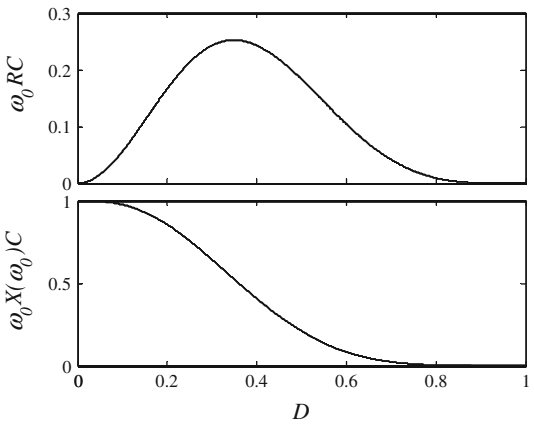

Fig. 4 $\omega_0 RC$ and $\omega_0 X(\omega_0)C$ with respect to the duty ratio D

The DC input resistance of the Class-E amplifier, R_{DC}, is important to analyze the input current and input power. Combining (3), (20) and (26) gives R_{DC} as

$$R_{DC} = \frac{V_{DD}}{I_{DD}} = \frac{\alpha R}{\beta \sin\theta_X}. \quad (28)$$

From (28) the relationship between R/R_{DC} and D can be obtained, as shown in Fig. 5.

It can be found that R_{DC} decreases as D increases, and the main values of equivalent DC input resistance R_{DC} and the input power P_{in} with respect to duty ratio D are shown in Table 1.

The load quality factor Q_L is defined as

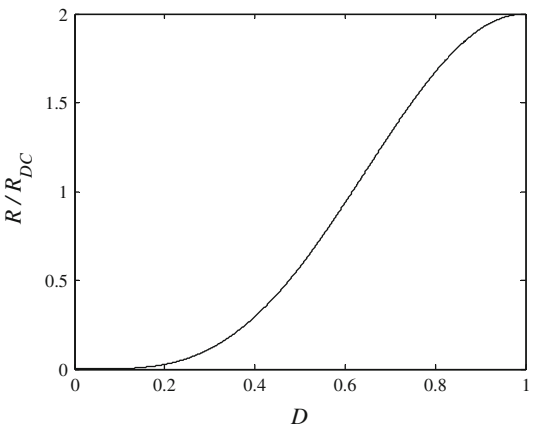

Fig. 5 R/R_{DC} with respect to duty ratio D

Table 1 R_{DC}, P_{in} and P_{out} with respect to duty ratio D

Parameters	D			
	0	0.5	0.62	1
R_{DC}	∞	$1.73R$	R	$0.5R$
P_{in}	0	$0.58P^{a}$	P^{a}	$2P^{a}$
P_{out}	0	$0.58P^{a}$	P^{a}	$2P^{a}$

[a] $P = V_{DD}^2/R$

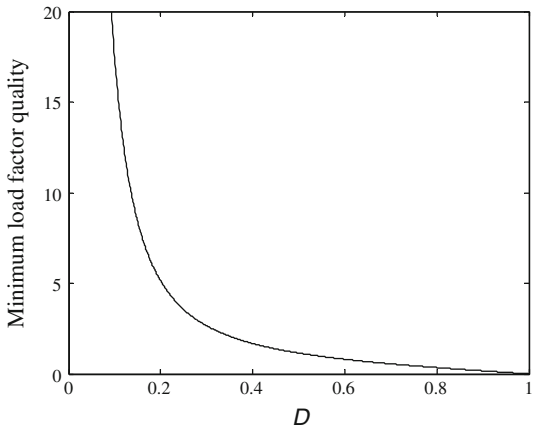

Fig. 6 Minimum load quality factor with respect to the duty ratio D

$$Q_L = \frac{\omega_0 L_1}{R}. \tag{29}$$

Since the parameter of capacitance C_1 is nonnegative, from (26), (27) and (29), the load quality factor Q_L is obtained to satisfy the inequality in terms of β and γ as

$$Q_L > \frac{X(\omega_0)}{R} = \frac{\gamma}{\beta}. \tag{30}$$

Figure 6 shows the minimum load quality factor $Q_{L\min}$ as a function of the duty rate D. $Q_{L\min}$ is a monotone decreasing function of D. However, as the assumption of high Q cannot be satisfied, a reasonable error exists between $Q_{L\min}$ and the actual minimal load quality factor. The minimal quality factor of the load network $Q_{L\min}$ reflects the practical one. Hence, it needs to set a large load quality factor Q_L when the duty ratio is small.

The input power and output power are determined by the following derivations. From (20) and (26), the amplitude of the output current can be expressed as

$$I_m = \frac{\beta V_{DD}}{\alpha R}. \tag{31}$$

Combining (3), (20), (26) and (31) gives the input power:

$$P_{in} = V_{DD} I_{DD} = \frac{\beta \sin\theta_X}{\alpha} \frac{V_{DD}^2}{R}. \tag{32}$$

Combining (20), (26) and (31) gives the output power:

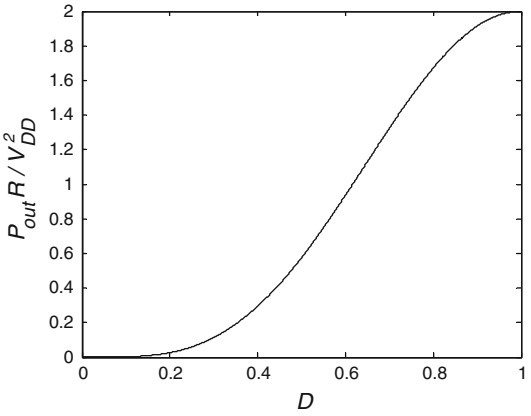

Fig. 7 $P_{out}R/V_{DD}^2$ with respect to duty ratio D

$$P_{out} = \frac{1}{2} I_m^2 R = \frac{\beta^2}{2\alpha^2} \frac{V_{DD}^2}{R}. \tag{33}$$

Figure 7 shows $P_{out}R/V_{DD}^2$ with respect to D. P_{out} increases as D increases. The main values of P_{out} are shown in Table 1.

The collect efficiency is

$$\eta_c = \frac{P_{out}}{P_{in}} = \frac{\beta}{2\alpha \sin\theta_X} = 1. \tag{34}$$

However, the efficiency is not 100% due to the resistance of every component of the Class-E amplifier. It is a tough work to calculate the accurate component parameters and efficiencies of a Class-E amplifier when the equivalent series resistance (ESR) is considered. It is reasonable to calculate the efficiency according to the results from the ideal analysis. Compared with the equivalent series resistance (ESR) of other components of Class-E amplifier, the on-resistance of the switch r_{on} is the main component contributing to the power loss. According to (31), the average power of r_{on} is

$$P_{r_{on}} = \frac{1}{2\pi} \int_{\theta_k''}^{\theta_k''+\theta_D} i_S^2(\theta) R_{on} d\theta = \frac{1}{2\pi} \frac{\beta^2 R_{on}}{\alpha^2 R} \delta \frac{V_{DD}^2}{R} \tag{35}$$

where

$$\delta = \theta_D \left(\frac{1}{2} + \sin^2\theta_X \right) + 2\sin\theta_X [\cos\theta_X - \cos(\theta_X - \theta_D)] - \frac{1}{4} [\sin 2\theta_X - \sin 2(\theta_X - \theta_D)] \tag{36}$$

From (32) and (35), the ratio of $P_{r_{on}}$ to P_{in} is

$$\eta_{r_{on}} = \frac{P_{r_{on}}}{P_{in}} = \frac{\beta \delta r_{on}}{2\pi\alpha \sin\theta_X R}. \tag{37}$$

Figure 8 shows $\eta_{r_{on}} R/r_{on}$ with respect to the duty ratio D. $\eta_{r_{on}}$ increases as D increases. The ratio of power loss

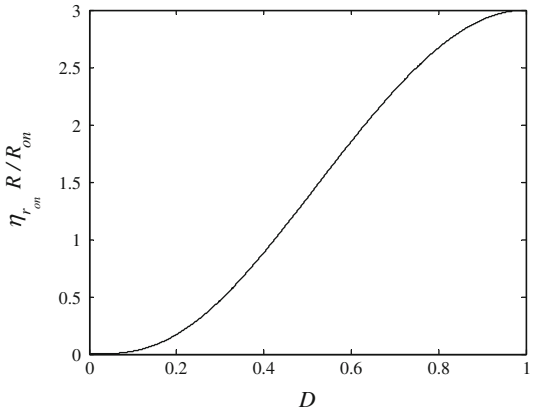

Fig. 8 $\eta_{r_{on}} R/r_{on}$ with respect to duty ratio D

in r_{on} over the input power P_{in} increases as D increases, consequently, the efficiency decreases.

4 Design procedure

Two design procedures are provided with the following design requirements: (1) The DC supply voltage V_{DD} is required. (2) The output power P_{out} and the collect efficiency η_c are required. In each procedure, the given parameters are the operating frequency f, switch ratio D, load resistance R, load quality Q.

Steps for the procedure (1):

(1) Calculate the phase difference θ_X by (11), and then calculate α, β, γ, δ with θ_D and θ_X;
(2) Calculate L_1 by (29) in terms of the given parameters R, Q, f;
(3) Calculate the shunt capacitance C by (26);
(4) Calculate C_1 by (27);
(5) Calculate choke coil by the formula $L_{RFC} = 2(\pi^2/4 + 1)R/f$ [9].
(6) Calculate the input power and efficiency with the DC supply voltage V_{DD} by (32) and (37), respectively.

Steps for the procedure (2):

Steps (1–5) are the same as those of the procedure (1).

(7) Calculate the maximum switch-on resistance of r_{on} with the ratio $\eta_{r_{on}} = 1 - \eta_c$ by (37), and then select a MOSFET with r_{on} smaller than the maximum one.

Calculate the supply voltage V_{DD} by (32) where $P_{in} = P_{out}/\eta_c$.

5 Simulations and experiments

From the design procedure (1) presented in Part IV, given the circuit parameters $f = 1$ MHZ, $V_{DD} = 6$ V, R = 10 Ω and $Q = 10$, the design parameters of the Class-E amplifier at three duty ratios, i.e. $D = 0.25$, 0.5 and 0.75, are calculated and shown in Table 2.

Table 2 Calculated parameters of the Class-E amplifier at $D = 0.25$, 0.5 and 0.75

D	L (μH)	C (nF)	L_1 (μH)	C_1 (nF)
0.25	69.35	3.39	15.92	2.47
0.5	69.35	2.92	15.92	1.80
0.75	69.35	0.35	15.92	1.67

With the three sets of parameters, the circuit shown in Fig. 1 was simulated with PSpice. The MOSFET was substituted by an switch component "IRF 510", which was driven by a square wave generated by the component "Vpulse". The Vpulse was set to 6 V amplitude, zero rise time, zero fall time and zero delay time.

Substituting R = 10 Ω and $r_{on} = 0.54$ Ω (per data sheet) into (37), the calculated collect efficiencies with respect to D were calculated and compared with simulated ones, as shown in Fig. 9. The simulated results agree well with the calculated ones when D is between 0.2 and 0.8. However, this agreement cannot be obtained at very small or large D.

In the simulation the voltage v_S and v_o take some time from their transient states to their steady states. The voltage waveform in the period between 98 and 100 μs is shown in Fig. 10(a–c). The values of the main parameters in the simulation are shown in Table 3. However, there are some differences due to the switch-on resistance r_{on}. The differences are smaller when duty ratio D is 0.5 than these when is 0.25 or 0.75.

In the experiment the MOSFET IRF 510 was used as the switch device, and the driving square waves were gained from ATMEGA 16 microcontroller. The choke coil was set

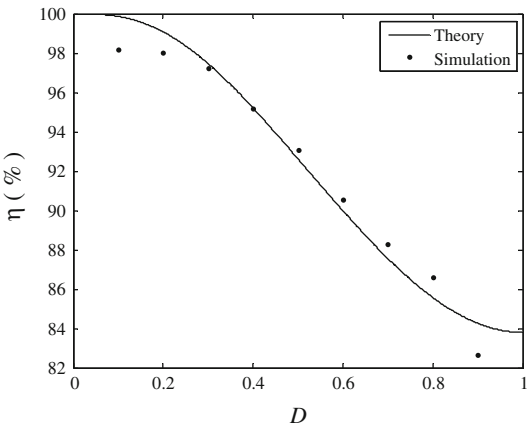

Fig. 9 Comparison of the simulation and theoretical values of the efficiency as function of the duty ratio D

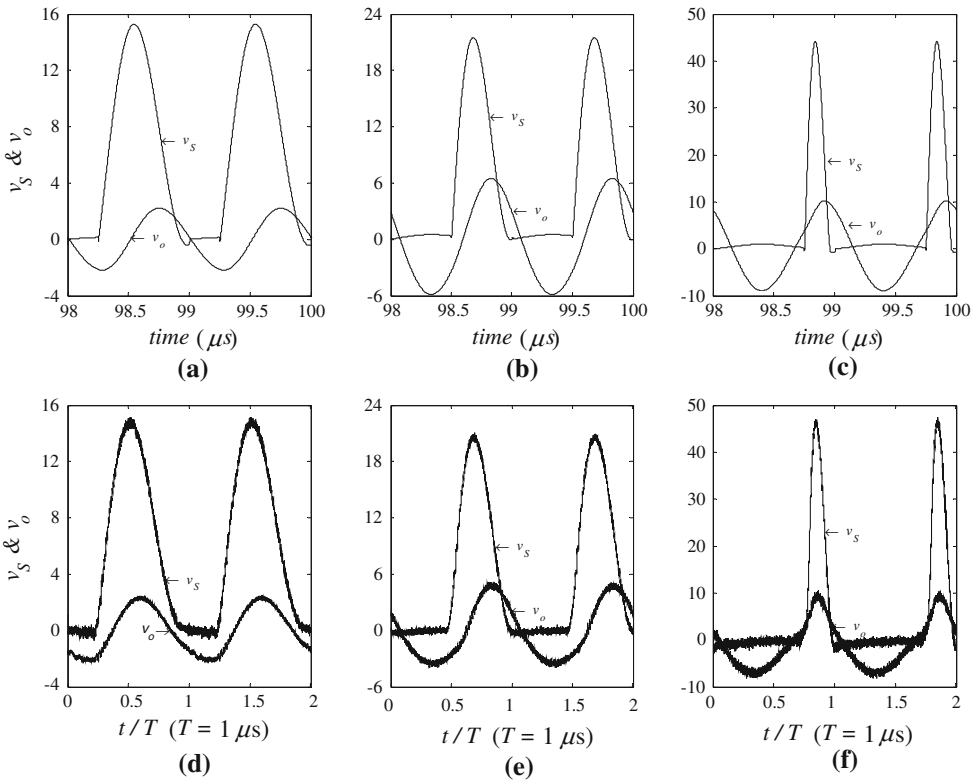

Fig. 10 Simulated and experimental waveforms of the switch voltage v_s and the output voltage v_o. **a** Simulation result at $D = 0.25$. **b** Simulation result at $D = 0.5$. **c** Simulation result at $D = 0.75$. **d** Experimental result at $D = 0.25$. **b** Experimental result at $D = 0.5$. **c** Experimental result at $D = 0.75$

Table 3 Calculated, simulated and experimental results of the Class-E amplifier at $D = 0.25$, 0.5 and 0.75

D	Parameters	Calculated	Simulation	Experimental
0.25	V_S (V)	17.9	15.3	14.6
	V_o (V)	2.1	2.3	2.2
	I_{DD} (mA)[a]	35.7	41.0	44
	η (%)	98.4	98.2	91
0.5	V_S (V)	24.6	21.5	20.8
	V_o (V)	6.4	6.5	5.0
	I_{DD} (mA)[a]	346.1	342.6	242
	η (%)	92.6	92.7	86
0.75	V_S (V)	42.3	40.0	46.0
	V_o (V)	10.4	9.7	9.0
	I_{DD} (mA)[a]	905.1	808.9	844
	η (%)	86.5	87.2	80

[a] Average value of the input current

to be 130 μH (approximately two-times larger than the calculated one) to reduce the impulse current through the switch when the power turns on. The equivalent series resistance (ESR) of the inductor L_1 in the loaded branch was 0.6 Ω, and the other components were taken as ideal components. The voltage v_S and v_o in the experiment are shown in Fig. 10(d–f). The values of the main parameters are shown in Table 2. Considering the ESR of each component, some differences among the experimental, simulation and calculated results will exist.

6 Conclusion

This paper presents a frequency-domain method for the analysis and design of Class-E amplifiers at any duty ratio D. According to the design analysis, as D increases, the DC input resistance decreases, and consequently the output power increases while the collect efficiency decreases. Based on these consequences, two design procedures for different purposes are presented with the design examples at $D = 0.25$, 0.5 and 0.75. The simulated and experimental results show that the differences of the switch voltage, output voltage, and the input and out power are less than 20%.

References

1. Sokal, N. O., & Sokal, A. D. (1975). Class E, a new class of high efficiency tuned singled-ended switching power amplifiers. *IEEE Journal of Solid-state Circuits, SC-10*(3), 168–176.
2. Sekiya, H., Nemoto, S., Lu, J. M., & Yahagi, T. (2006). Phase control for resonant DC-DC converter with Class-DE inverter and Class-E rectifier. *IEEE Transactions on Circuits and System, 53*(2), 254–263.
3. Hasani, J. Y., & Kamarei, M. (2008). Analysis and optimum design of a Class-E RF power amplifier. *IEEE Transactions on Circuits and Systems I-Regular Papers, 55*(6), 1759–1768.
4. Raab, F. H. (1977). Idealized operation of the Class E tuned power amplifier. *IEEE Transactions on Circuits and Systems, CAS-24*(12), 725–735.

5. Kazimierczuk, M. K., & Puczko, K. (1987). Exact analysis of Class E tuned power amplifier at any Q and switch duty cycle. *IEEE Transactions on Circuits and Systems, CAS-34*(2), 149–159.
6. Sokal, N. O. (2001). Class-E RF power amplifiers. *QEX*, 9–20.
7. Suetsugu, T., & Kazimierczuk, M. K. (2006). Design procedure of Class-E amplifier for off-nominal operation at 50% duty ratio. *IEEE Transactions on Circuits and Systems, 53*(7), 1468–1476.
8. Suetsugu, T., & Kazimierczuk, M. K. (2007). Off-nominal operation of Class-E amplifier at any duty ratio. *IEEE Transactions on Circuits and Systems, 54*(6), 1389–1397.
9. Kazimierczuk, M. K., & Czarkowski, D. (1995). *Resonant power converters*. New York: Wiley.

Tianliang Yang received the B.S. degree in Electrical Engineering and M.S. in Mechatronics Engineering from Nanchang Hangkong University, Nanchang, China, in 2003 and 2006, respectively. Currently he is working toward the Ph.D. degree in Electrical Engineering at Shanghai Jiao Tong University. His research interests include power amplifier, dc/dc converters, wireless power and data transfer, implantable electronics and smart telemetry.

Junrui Liang received the B.S. and M.S. degrees in Instrumentation Engineering from Shanghai Jiao Tong University, Shanghai, China, in 2004 and 2007, respectively, and the Ph.D. degree in Mechanical and Automation Engineering from the Chinese University of Hong Kong, Hong Kong, China, in 2010. His research interests include piezoelectric energy harvesting, Class-E power amplifier, and wireless power transmission.

Chunyu Zhao received the Ph.D. degree from Shanghai Jiao Tong University, Shanghai, China, in 2000. Currently he is an Associate Professor of the Department of Instrument Science and Engineering at Shanghai Jiao Tong University. His research interests include prosthetic devices, power amplifier, dc/dc converters and inductive links, neural-electronic interfaces and wireless biotelemetry.

Dayue Chen received the Ph.D. degree from Shanghai Jiao Tong University, Shanghai, China, in 1989. Currently, Prof. Chen is the Director of Institute of Intelligent Mechatronics Research of Shanghai Jiao Tong University. His research interests include prosthetic devices, neural-electronic interfaces, implantable electronics, inductive link, and smart telemetry.