An Improvement on Extended Impedance Method towards Efficient Steady-State Analysis of High-Frequency Class-E Resonant Inverters

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***Abstract*—The extended impedance method (EIM) is an efficient and intuitive tool for the design and analysis of power switching circuits with active components, nonlinear parasitic components, etc., under high-frequency operation. In this paper, we propose an improvement to the EIM by simplifying the constitutive circuit equations in the iterative calculation, such that to speed up the steady-state searching process. Taking the class-E resonant inverter, which is driven by a practical MOSFET switch, as the testbed, we comparatively evaluate the computational efforts of this improved EIM, the conventional EIM, and PSpice simulation, under the same circuit conditions. The result shows that the proposed method can greatly reduce the simulation time. Therefore, the improved EIM can be used as an efficient tool for the analysis, design, and optimization of high-frequency power electronics.**

I. Introduction

Nowadays, in different studies of power electronics, there is an obvious trend working towards the high-frequency and high-power-density power converters. One of the driving force is the popularization of the high-speed switching semiconductors, such as SiC and GaN; the other is the demand of more compact and more capable power converters. For example, in the wireless power transfer systems, by raising the switching frequency from several hundred kHz [1] to several MHz [2]–[4], the power density of the circuit can be increased; the size of passive components can be reduced.

The single-ended class-E resonant inverter, which is also called class-E power amplifier (PA), was proposed in 1975 [5], [6]. It is known for its simple structure, high efficiency, and high-frequency operation. In the old days, when the switching frequency is as low as several hundred kHz, the nonlinearity of the parasitic components can be neglected. The design of class-E PA usually starts with the circuit equations and waveform equations in the time-domain [7]–[10]. As the switching frequency gets higher, the electrical susceptance of the nonlinear junction capacitor in the switching transistor becomes larger and dominant in the shunt capacitance. In such high-frequency scenario, the effect of nonlinear parasitic components, as well as other large-signal behavior, must receive sufficient consideration in the design and analysis of power converters [11].

Analytical waveform solutions provide intuitions towards the conceptual design [5]. However, the closed-form equations

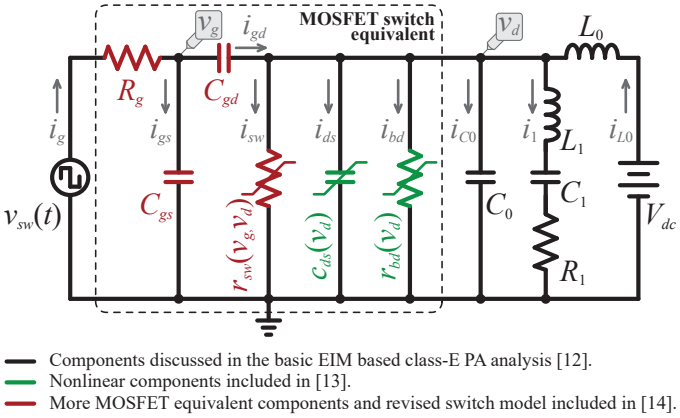


Fig. 1. Equivalent model of the class-E resonant inverter considering the MOSFET parasitic components.

can hardly express all the details in practical circuits, in particular, when the effect of parasitic components in semiconductor becomes significant and non-ignorable. Numeric simulation or analysis are complementary design techniques towards the detailed performance. The numeric design methods can be classified into time-domain methods [1] and frequency-domain methods [12]–[14].

The extended impedance method (EIM) [12]–[14] was proposed for realizing the steady-state design numerically around the linear specifications, which are obtained with the established method [6]. The harmonic based EIM is different from the conventional harmonic balance method. In EIM, the characteristics of all time-varying and nonlinear components are regarded as special impedances, whose algorithm of combination is compatible with the fundamental linear ac circuit analysis. Therefore, it is more intuitive towards nonlinear circuit analysis.

This paper discusses an improvement to the EIM based on the modified nodal analysis (MNA) towards a more efficient design process of class-E PA under high-frequency operation.

II. Theory

The equivalent model of class-E PA using practical MOSFET switch is shown in Fig. 1 [14]. V_{dc}, L_0, and C_0 are the dc supply voltage, choke inductance, and shunt capacitance,

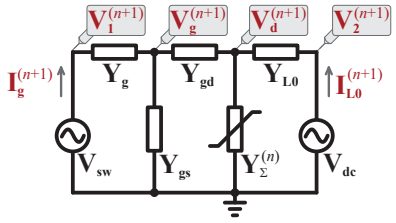


Fig. 2. Simplified circuit network for modified nodal analysis (MNA).

respectively. R_1, C_1, and L_1 form the resonant branch. The components within the dashed frame forms the equivalent of a practical MOSFET. c_{ds} and r_{bd} represent the nonlinear drain-to-source junction capacitance and body diode, respectively, whose effects under different operations were discussed in [13]; R_g, C_{gs}, C_{gd}, and r_{sw} are the gate resistance, gate-to-source capacitance, gate-to-drain capacitance, and switching resistance, respectively, whose effects under different gate drive voltage were discussed in [14]. V_{sw} provides the gate drive to the MOSFET.

Since all the components in Fig. 1 can be regarded as impedances, whose expressions have been extended from complex scalars to complex matrices [12]. The constitutive circuit equations can be obtained according to the conventional laws in linear network analysis, e.g., KCL, KVL. Such network was successfully formulated by using the loop current method in [14]. After [14], research effort has been continuously made with the following two purposes:

1) Make the EIM based analysis more compatible to the established circuit simulation program, e.g., SPICE, such that the netlist file SPICE can be readily reused in the EIM based solver.
2) Further reduce the computational effort of EIM, in particular, in the iterative state-update procedure.

As the modified nodal analysis (MNA) is extensively used in formulating the circuit network in most existing simulation program [15], such as SPICE, this paper adopts the MNA for formulating the constitutive circuit equations as follows

$$\begin{bmatrix} \mathbf{V_1}^{(n+1)} \\ \mathbf{V_g}^{(n+1)} \\ \mathbf{V_d}^{(n+1)} \\ \mathbf{V_2}^{(n+1)} \\ \mathbf{I_g}^{(n+1)} \\ \mathbf{I_{L0}}^{(n+1)} \end{bmatrix} = \begin{bmatrix} \mathbf{Y_g} & -\mathbf{Y_g} & \mathbf{0} & \mathbf{0} & \mathbf{E} & \mathbf{0} \\ -\mathbf{Y_g} & \mathbf{Y_{\Sigma g}} & -\mathbf{Y_{gd}} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & -\mathbf{Y_{gd}} & \mathbf{Y_{\Sigma d}}^{(n)} & -\mathbf{Y_{L0}} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & -\mathbf{Y_{L0}} & \mathbf{Y_{L0}} & \mathbf{0} & \mathbf{E} \\ \mathbf{E} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} & \mathbf{E} & \mathbf{0} & \mathbf{0} \end{bmatrix}^{-1} \begin{bmatrix} \mathbf{0} \\ \mathbf{0} \\ \mathbf{0} \\ \mathbf{0} \\ \mathbf{V_{sw}} \\ \mathbf{V_{dc}} \end{bmatrix}, \tag{1}$$

TABLE I
PARAMETERS IN THE CASE STUDIES OF CLASS-E PA.

Parameter	Value
V_{dc}	20 V
V_{sw} [amp. of $v_{sw}(t)$]	±7.0 V
f_{sw} [freq. of $v_{sw}(t)$]	6.78 MHz
D	50 %
L_0	100 μH
C_0	132.35 pF
L_1	1.03 μH
C_1	757.78 pF
R_1	10.03 Ω
MOSFET	IRF510

The circuit parameters are obtained based on the revised design equations in [6]. The IRF510 specifications were provided in [14].

where

$$\mathbf{Y_{\Sigma g}} = \mathbf{Y_g} + \mathbf{Y_{gs}} + \mathbf{Y_{gd}}, \tag{2}$$

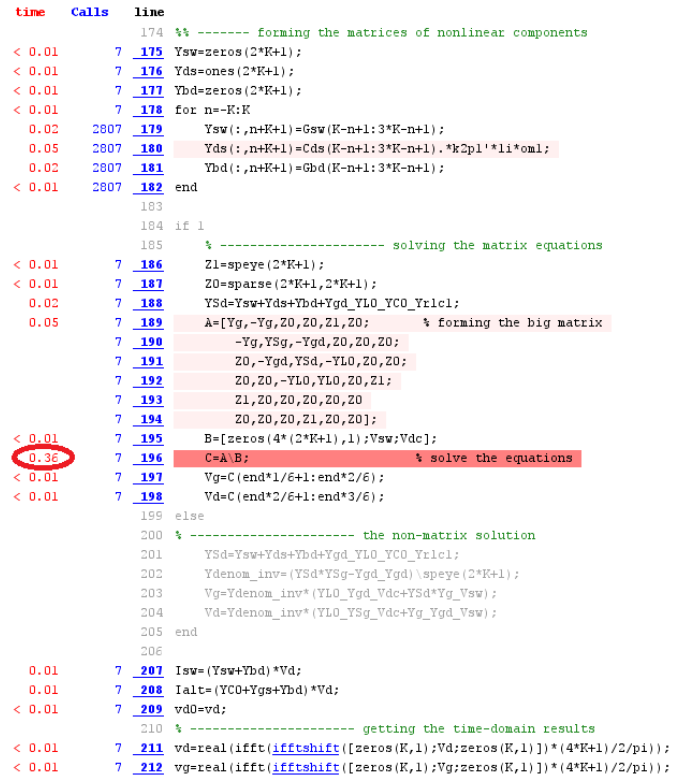
$$\mathbf{Y_{\Sigma d}}^{(n)} = \mathbf{Y_{gd}} + \mathbf{Y_\Sigma}^{(n)} + \mathbf{Y_{L0}}, \tag{3}$$

$$\mathbf{Y_\Sigma}^{(n)} = \mathbf{Y_{sw}}^{(n)} + \mathbf{Y_{ds}}^{(n)} + \mathbf{Y_{bd}}^{(n)} + \mathbf{Y_{C0}} + (\mathbf{Z_{R1}} + \mathbf{Z_{C1}} + \mathbf{Z_{L1}})^{-1}. \tag{4}$$

The relations are obtained according to the simplified circuit network shown in Fig. 2. The four voltage nodes other than the ground are denoted as the vectors $\mathbf{V_1}$, $\mathbf{V_g}$, $\mathbf{V_d}$, and $\mathbf{V_2}$. The dc supply and gate drive voltage are taken as two general voltage sources, whose flowing-through currents are $\mathbf{I_g}$ and $\mathbf{I_{L0}}$, respectively. The superscript $(n+1)$ denote the results in the $(n+1)$th iteration. The corresponding admittance in the matrix of (1) is shown in Fig. 2. The voltage and current vectors, whose dimensions are $(2K+1)\times 1$, express the circuit states in the frequency domain with a harmonic number of K; the matrices, whose dimensions are $(2K+1)^2$, express the characteristics of the components in the form of admittances. Within those admittances, $\mathbf{Y_\Sigma}$ is the only nonlinear one. As we can observed from Fig. 1 and (4), the nonlinearities come from the MOSFET switching, whose characteristic is denoted by $\mathbf{Y_{sw}}$, drain-to-source junction capacitance denoted by $\mathbf{Y_{ds}}$, and body diode denoted by $\mathbf{Y_{bd}}$.

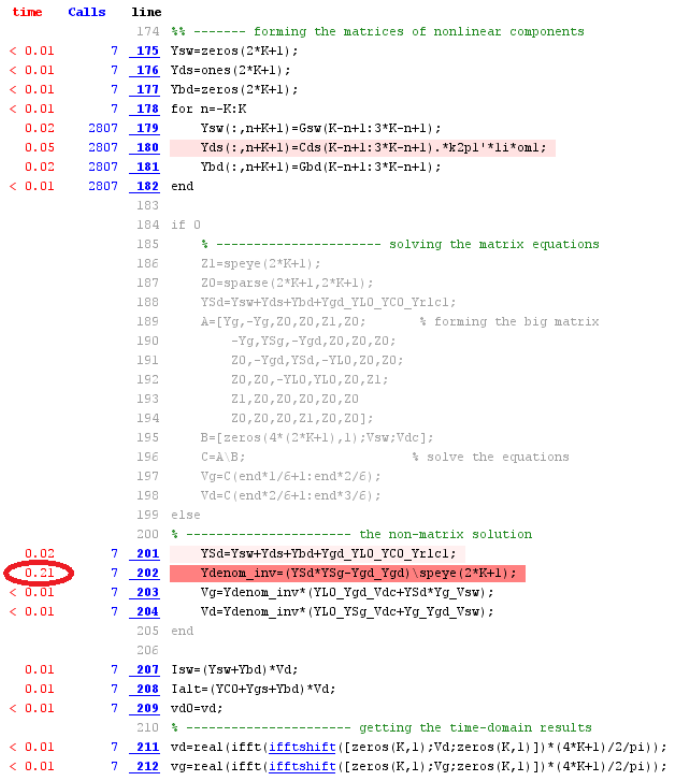
With (1), the four voltage and two current unknowns can be immediately solved by doing the matrix inversion. A Matlab program is developed based on the sparse matrix manipulations for simulating a class-E PA, whose specifications are listed in Table I. The execution summary by using full matrix inversion algorithm is shown in Fig. 3. It can be observed from Fig. 3 that the matrix inversion takes the longest time to execute compared to other lines.

On the other hand, in the six unknown voltages and currents, actually only $\mathbf{V_g}^{(n+1)}$ and $\mathbf{V_d}^{(n+1)}$ are useful information for updating the admittance matrices $\mathbf{Y_{sw}}^{(n+1)}$, $\mathbf{Y_{ds}}^{(n+1)}$, and $\mathbf{Y_{bd}}^{(n+1)}$ in the next round of calculation. A approximating solution can be formulated by taking the matrix in (1) as a 6×6 block



time	Calls	line	
		174	%% ------- forming the matrices of nonlinear components
< 0.01	7	175	Ysw=zeros(2*K+1);
< 0.01	7	176	Yds=ones(2*K+1);
< 0.01	7	177	Ybd=zeros(2*K+1);
< 0.01	7	178	for n=-K:K
0.02	2807	179	Ysw(:,n+K+1)=Gsw(K-n+1:3*K-n+1);
0.05	2807	180	Yds(:,n+K+1)=Cds(K-n+1:3*K-n+1).*k2pl'*1i*oml;
0.02	2807	181	Ybd(:,n+K+1)=Gbd(K-n+1:3*K-n+1);
< 0.01	2807	182	end
		183	
		184	if 1
		185	% ---------------------- solving the matrix equations
< 0.01	7	186	Z1=speye(2*K+1);
< 0.01	7	187	Z0=sparse(2*K+1,2*K+1);
0.02	7	188	YSd=Ysw+Yds+Ybd+Ygd_YL0_YC0_Yrlc1;
0.05	7	189	A=[Yg,-Yg,Z0,Z0,Z1,Z0; % forming the big matrix
	7	190	-Yg,YSg,-Ygd,Z0,Z0,Z0;
	7	191	Z0,-Ygd,YSd,-YL0,Z0,Z0;
	7	192	Z0,Z0,-YL0,YL0,Z0,Z1;
	7	193	Z1,Z0,Z0,Z0,Z0,Z0
	7	194	Z0,Z0,Z0,Z1,Z0,Z0];
< 0.01	7	195	B=[zeros(4*(2*K+1),1);Vsw;Vdc];
0.36	7	196	C=A\B; % solve the equations
< 0.01	7	197	Vg=C(end*1/6+1:end*2/6);
< 0.01	7	198	Vd=C(end*2/6+1:end*3/6);
		199	else
		200	% ---------------------- the non-matrix solution
		201	YSd=Ysw+Yds+Ybd+Ygd_YL0_YC0_Yrlc1;
		202	Ydenom_inv=(YSd*YSg-Ygd_Ygd)\speye(2*K+1);
		203	Vg=Ydenom_inv*(YL0_Ygd_Vdc+YSd*Yg_Vsw);
		204	Vd=Ydenom_inv*(YL0_YSg_Vdc+Yg_Ygd_Vsw);
		205	end
		206	
0.01	7	207	Isw=(Ysw+Ybd)*Vd;
0.01	7	208	Ialt=(YC0+Ygs+Ybd)*Vd;
< 0.01	7	209	vd0=vd;
		210	% ---------------------- getting the time-domain results
< 0.01	7	211	vd=real(ifft(ifftshift([zeros(K,1);Vd;zeros(K,1)])*(4*K+1)/2/pi));
< 0.01	7	212	vg=real(ifft(ifftshift([zeros(K,1);Vg;zeros(K,1)])*(4*K+1)/2/pi));

Fig. 3. The execution time of the Matlab program (harmonic no. $K = 200$) based on the full matrix inversion EIM algorithm (the deeper red the highlighting line, the more time for the execution).



time	Calls	line	
		174	%% ------- forming the matrices of nonlinear components
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< 0.01	7	178	for n=-K:K
0.02	2807	179	Ysw(:,n+K+1)=Gsw(K-n+1:3*K-n+1);
0.05	2807	180	Yds(:,n+K+1)=Cds(K-n+1:3*K-n+1).*k2pl'*1i*oml;
0.02	2807	181	Ybd(:,n+K+1)=Gbd(K-n+1:3*K-n+1);
< 0.01	2807	182	end
		183	
		184	if 0
		185	% ---------------------- solving the matrix equations
		186	Z1=speye(2*K+1);
		187	Z0=sparse(2*K+1,2*K+1);
		188	YSd=Ysw+Yds+Ybd+Ygd_YL0_YC0_Yrlc1;
		189	A=[Yg,-Yg,Z0,Z0,Z1,Z0; % forming the big matrix
		190	-Yg,YSg,-Ygd,Z0,Z0,Z0;
		191	Z0,-Ygd,YSd,-YL0,Z0,Z0;
		192	Z0,Z0,-YL0,YL0,Z0,Z1;
		193	Z1,Z0,Z0,Z0,Z0,Z0
		194	Z0,Z0,Z0,Z1,Z0,Z0];
		195	B=[zeros(4*(2*K+1),1);Vsw;Vdc];
		196	C=A\B; % solve the equations
		197	Vg=C(end*1/6+1:end*2/6);
		198	Vd=C(end*2/6+1:end*3/6);
		199	else
		200	% ---------------------- the non-matrix solution
0.02	7	201	YSd=Ysw+Yds+Ybd+Ygd_YL0_YC0_Yrlc1;
0.21	7	202	Ydenom_inv=(YSd*YSg-Ygd_Ygd)\speye(2*K+1);
< 0.01	7	203	Vg=Ydenom_inv*(YL0_Ygd_Vdc+YSd*Yg_Vsw);
< 0.01	7	204	Vd=Ydenom_inv*(YL0_YSg_Vdc+Yg_Ygd_Vsw);
		205	end
		206	
0.01	7	207	Isw=(Ysw+Ybd)*Vd;
0.01	7	208	Ialt=(YC0+Ygs+Ybd)*Vd;
< 0.01	7	209	vd0=vd;
		210	% ---------------------- getting the time-domain results
< 0.01	7	211	vd=real(ifft(ifftshift([zeros(K,1);Vd;zeros(K,1)])*(4*K+1)/2/pi));
< 0.01	7	212	vg=real(ifft(ifftshift([zeros(K,1);Vg;zeros(K,1)])*(4*K+1)/2/pi));

Fig. 4. The execution time of the Matlab program (harmonic no. $K = 200$) based on the improved EIM algorithm (the deeper red the highlighting line, the more time for the execution).

matrix. By solving the six symbolic linear equations, we can obtain

$$\mathbf{V_g^{(n+1)}} \approx \left[\mathbf{Y_{\Sigma d}^{(n)} Y_{\Sigma g} - Y_{gd}^2}\right]^{-1} \left[\mathbf{Y_{L0} Y_{gd} V_{dc} + Y_g Y_{\Sigma d}^{(n)} V_{sw}}\right] \tag{5}$$

$$\mathbf{V_d^{(n+1)}} \approx \left[\mathbf{Y_{\Sigma d}^{(n)} Y_{\Sigma g} - Y_{gd}^2}\right]^{-1} \left(\mathbf{Y_{L0} Y_{\Sigma g} V_{dc} + Y_g Y_{gd} V_{sw}}\right) \tag{6}$$

It should point out that, from the fundamental principle of linear algebra, the expressions of (5) and (6) do not rigorously hold, as there might be cross-coupling terms across the blocks. Here, we do the approximation and try to use such method to reduce the computational effort towards the circuit optimization. The case study with the class-E specifications of Table I by using such approximation actually gives a similar voltages as that using the full matrix inversion (will be shown in the next section). On the other hand, as shown in Fig. 4, the most critical line in the new algorithm is also the matrix inversion step. Yet, the computational time of this critical line in the new program is about 58% of that in the full matrix solution. Therefore, by only calculating the useful information, the computation time can be further reduced towards more efficient EIM based analysis.

III. Design Procedures

An example design case is provided here for validating the waveform analysis of EIM, and also describing the design procedures with EIM based circuit optimization. Fig. 5 shows four testing circuits in the design procedures.

1) Obtain the component values with the conventional design laws or guidelines considering an ideal switch and linear components.
2) Replace the ideal switch with practical transistor model. Simulate the changes in operation.
3) Design the EIM based numerical optimization to approach the design objective, e.g., ZVS and ZCS in the class-E circuit, constant output power, or highest conversion efficiency.
4) Simulate the re-tuned parameters and comparatively evaluate the design feasibility.

The results in Fig. 6 show that the class-E nominal ZCS condition is violated when the ideal switch model (whose result is shown by the dash-dot-dot lines) is replaced by a practical MOSFET model (whose result is shown by the solid lines).

Owing to the high computational efficiency of EIM, we manage to develop a derivative-free algorithm [12], [13] for re-tuning the nonlinear class-E circuit back to the vicinity of the nominal conditions. The full matrix optimization leads to the optimized capacitance pairs $C_0 = 411$ pF and $C_1 = 819$

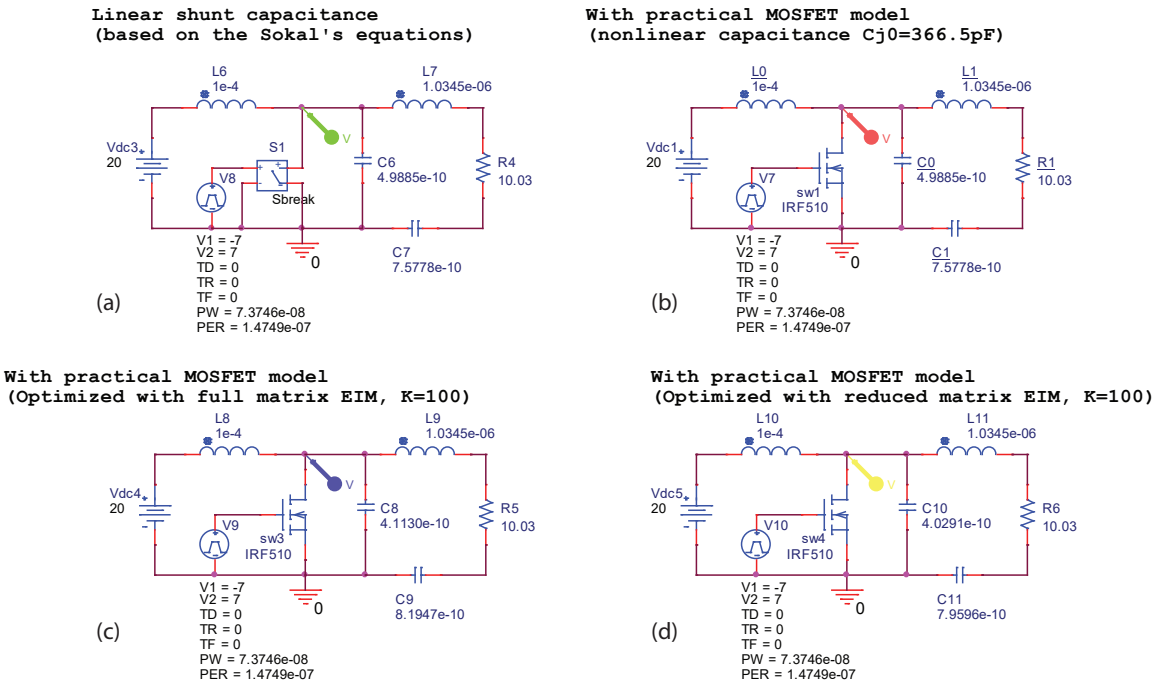

Fig. 5. Four testing conditions for the comparative study. (a) Class-E circuit with linear shunt capacitance and ideal switch. (b) The ideal switch is replaced by a MOSFET model. (c) Re-tuned circuit with full matrix EIM ($C_0 = 411$ pF, $C_1 = 819$ pF). (d) Re-tuned circuit with reduced matrix EIM ($C_0 = 403$ pF, $C_1 = 796$ pF).

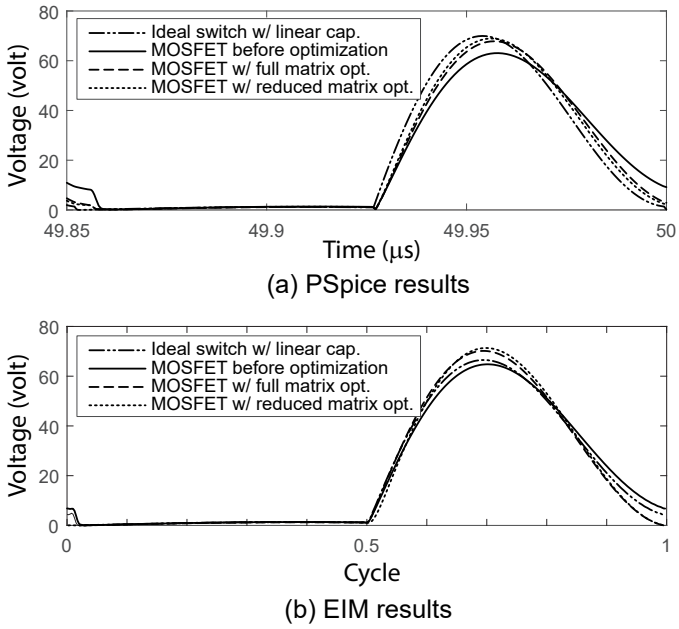

Fig. 6. Simulation waveforms obtained with PSpice and EIM.

pF, as illustrated in Fig. 5(c); the waveform result is shown by the dash lines in Fig. 6. It shows that the ZVS and ZDS conditions are recovered under the tuned C_0 and C_1. The reduced matrix optimization leads to another optimized capacitance pair $C_0 = 403$ pF and $C_1 = 796$ pF, which are very close to the full matrix optimization results. The waveforms obtained under the two optimization algorithm are very close and almost overlap in Fig. 6(b). Both the full matrix and reduced matrix can successfully fulfill the designed task.

IV. Conclusion

This paper has considered a possible improvement on the extended impedance method (EIM) towards the more efficient frequency-domain simulation and optimized design of high-frequency and high-power-density power electronics. In the class-E circuit example, since only the gate and drain voltages have an effect over the nonlinear parasitic components in the switching transistor, the execution time can be reduced by eliminating the other useless information during the iterative state update process. The performance evaluator in Matlab shows the superiority of the proposed improvement towards the customized analyses and designs of power electronics.

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