Series Synchronized Triple Bias-flip (S-S3BF) Interface Circuit for Piezoelectric Energy Harvesting

Kang Zhao, Junrui Liang, and Haoyu Wang School of Information Science and Technology ShanghaiTech University, Shanghai 201210, China Email: liangjr@shanghaitech.edu.cn

Abstract—This paper introduces the series synchronized triple bias-flip (S-S3BF) interface circuit for piezoelectric energy harvesting (PEH) enhancement. The S-S3BF topology is derived from its parallel counterpart (P-S3BF), which was proved to offer the maximum energy harvesting capability when three bias-flip actions are implemented. The S-S3BF is a little bit less capable than P-S3BF. However, it eliminates the circuit components by removing the bridge rectifier connected in parallel, such that can use only one capacitor to realize the bias voltages and energy storage simultaneously. Compared to the other single capacitor designs, the S-S3BF makes the best energy harvesting capability so far. Moreover, S-S3BF can automatically shift among single, double, and triple bias-flip operations under heavy, medium, and light load conditions, respectively. Therefore, it is more adaptive than previous designs. Theoretical and experimental results show that the harvested power can always follow the envelope (best case) of the single, double, and triple bias-flip operations during an entire charging process.

I. INTRODUCTION

The power supply issue of the dispersively distributed electronic devices has become one of the most significant constraints for their deployment and also significantly increased their maintenance cost after the installation. Scavenging energy from the ambient vibrations has been investigated as one of the promising solutions to this problem. Among all kinds of electromechanical transducers, the piezoelectric one provides the simplest mechanical structure for making an energy harvesting system. Therefore, it has caught extensive research interest during the last decade [1]. Researchers working on piezoelectric energy harvesting (PEH) are mainly focused on three aspects, piezoelectric materials (higher power density) [2], mechanical structures [3], and power conditioning circuits. Fig. 1(a) shows the cantilevered beam structure, which is widely discussed in PEH studies. The piezoelectric transducers are glued near the fixed end of the cantilevered structure, where maximum strain exists. An interface circuit is connected to the two electrodes of the piezoelectric element, such that to condition the piezoelectric voltage and the output energy. Fig. 1(b) is the equivalent electrical model of the piezoelectric system. v_{pz} is proportional to the excitation force; R, L, and C represent the damping, mass, and stiffness of the mechanical structure; C_p and R_p are the clamped capacitor and leakage resistance. The mechanical properties can be characterized by an impedance analyzer [4].

Since the start of research interest on PEH, various circuit topologies have been proposed for better conditioning of the



Fig. 1. PEH system. (a) Mechanical configuration. (b) Equivalent electrical model.

harvested power [1]. The most convenient way for ac-to-dc conversion is to use a bridge rectifier, which was regarded as the standard energy harvesting (SEH) interface circuits. Later studies have introduced the synchronized switching resistance inductance and capacitance (RLC) transient for enlarging the energy harvesting capability, e.g., the synchronized switch harvesting on inductor (SSHI) and the synchronous electric charge extraction (SECE). The emergence of the concepts of "active energy harvesting" [5], "energy investment" [6], "energy injection" [7], and "pre-biasing" [8] has brought new ideas for further energy harvesting enhancement. However, the previous designs request complex control, additional adaptive sources, etc. The followers are rare. Liang et al. have theoretically derived the optimal energy investment strategy [9] based on the generalized synchronized multiple bias-flip (SMBF) model. They later implemented the parallel and M = 3 version of SMBF (P-S3BF) [10] and P-S7BF [11]. Recently, there are some multiple voltage-jump designs reported from the integrated circuit (IC) community [12]-[14], all of which were based on the switched-capacitor principle. Given the same number of voltage jumps; the harvestable power can be higher by using the inductive bias-flipping designs [9].

In most of the multiple bias-flip designs, additional auxiliary capacitors and a current steering switch network are necessary for realizing the SMBF control. Those additional component



Fig. 2. S-S3BF circuit topology.

increases the complexity of the power conditioning circuit or even bring some uncertainty to the system. In this paper, we investigate how to make the furthest reuse of a single capacitor as the energy storage component and also the bias-voltage source.

II. CIRCUIT TOPOLOGY AND OPERATION

The earlier proposed P-S3BF and P-S7BF [10], [11] circuits were developed with the aim to achieve the maximum harvesting capability under the SMBF generalization, which includes both the parallel and series cases. Circuit simplicity was not the prior design consideration in those designs. In P-S3BF, three bias voltages are realized by reusing one additional capacitor; in P-S7BF, seven bias voltages are realized by reusing twos. Connecting the additional axillary capacitors bring a new problem that the circuit can attain the steady state after the axillary capacitors are charged to some certain levels, which was called the charging transient in [10], [11]. Therefore, compared to the single bias-flip counterparts, the P-SMBF implementations take more time to settle down.

It is curious that whether we can further eliminate the capacitive component and make the circuit simpler. The solution is not complicated. It can be achieved by just removing the bridge rectifier in the parallel path and integrate the energy storage function into the axillary capacitor. By doing so, the harvesting capability is sacrificed a little bit; yet, it makes the circuit more compact and be able to settle down faster.

Fig. 2 shows the circuit topology of S-S3BF. Under weakly coupling condition of constant magnitude vibration, the piezoelectric structure can be equivalently modeled as the parallel combination of three parts: the equivalent current source $i_{eq}(t)$, which is proportional to the vibration velocity; the piezoelectric clamped capacitance C_p ; and the shunt leakage resistance R_p . $i_{eq}(t)$ is regarded as the current flowing through the RLC circuit branch in Fig. 1(b) in resonance. The S-S3BF circuit implementation adopts the expandable current steering switch network configuration, which was used in the P-S7BF design [11]. The switch network is composed of eight power MOSFET and four diodes for properly controlling the current flow and direction in each bias-flip action. In each cell of switches, i.e., from M_{x1} to M_{x4} (x = 0, 1), the two transistors



Fig. 3. Waveforms, control sequence and operation phases of S-S3BF in half of a vibration cycle (downstairs). (a) Voltage and current overviews. (b) The enlarged view of the downstairs instant. (c)-(f) Control sequence in the downstairs half cycle. (c) Phase 1: open circuit. (d) Phase 2: the first bias-flip. (e) Phase 3: the second bias-flip. (f) Phase 4: the third bias-flip.

 TABLE I

 TRANSIENT STAGES AND THEIR CORRESPONDING EQUIVALENT FLIPPING

 FACTORS.

		Equivalent impping factor
Single bias-flip Double bias-flip Triple bias-flip 1	1^{st} 1^{st} , 3^{rd} 1^{st} , 2^{nd} , 3^{rd}	$\begin{array}{l} \gamma_1=\gamma,\gamma_2=\gamma_3=1\\ \gamma_1=\gamma_3=\gamma,\gamma_2=1\\ \gamma_1=\gamma_2=\gamma_3=\gamma \end{array}$

 γ is the actual flipping factor. Unit flipping factor means no bias-flip action

 M_{x1} and M_{x2} form a bidirectional switch; M_{x3} and D_{x3} form the upward current path; and M_{x4} and D_{x4} form the downward one. The capacitor C_b connects the middle points of the two switch branches. C_b is not only used to provide the bias-voltage references during each bias-flip action but also act as the energy storage and supply dc power to the load resistor R_l , which is connected in parallel to C_p .

By properly controlling the switching sequence at each synchronized instant (zero-crossing point of vibration velocity), a sophisticated current flow can be produced through C_p , such that triple continuous bias-flip actions can be realized. Fig. 3 shows the waveforms, control sequence, and half of the operation phases of S-S3BF. When the equivalent current i_{eq} is positive, the current steering network is shut down. The piezoelectric capacitance C_p is internally charged by i_{eq} and rises gradually, as shown in Fig. 3(a). At the same time, the capacitor C_b supplies dc power to the load resistor. This "open circuit" period is marked with "phase 1" in Fig. 3(a). Its corresponding conducting branches are shown in 3(c). Once the synchronized instant is reached, i.e., velocity or equivalent current i_{eq} crosses zero, the MOSFET switches will operate at the current steering network and carry out the three continues bias-flip actions, which are marked with "phase 2", "phase 3", and "phase 4" in Fig. 3(b). Their corresponding conducting branches are shown in 3(d), (e) and (f), respectively. Owing to the current steering diodes D_{x3} and D_{x4} (x = 0, 1) in the lower part of each branch, the actual bias voltages in the three bias-flip actions are $V_b + V_d$, V_d and $-V_b + V_d$, respectively, where V_b is the dc value, which approximates the slowly changing v_b ; V_d is the forward voltage drop of a diode. Fig. 3(b) shows the enlarged view of the voltage waveform at steady state. Besides these four phases under positive i_{eq} , there are other four phases from phase 5 to phase 8 under negative i_{eq} . The symmetric circuit branches will be conducted in sequence respectively to realize the three continuous rising bias-flip actions.

In the previously studied P-S3BF circuit, there is an "energy neutral" principle under steady state [10]. It means that the bias voltage v_b changes only at the synchronized instant, the amounts of absorbed and invested energy during the first and third bias-flip actions are the same. In other words, the bias voltage after three continuous bias-flip actions, i.e., $v_b(t_3)$, equals to that before the bias-flip actions, i.e., $v_b(t_0)$. Different from that, in S-S3BF, C_b also acts as the dc supply to power the load resistor R_l during the open-circuit phases, i.e., phase 1 and 5. the energy neutral condition is violated. The energy



Fig. 4. The charging curve of the bias/storage voltage V_b under three different loading conditions.

absorption must be larger than the back investment, such that we have $v_b(t_3) > v_b(t_0)$, as shown in Fig. 3(b).

III. ANALYSIS

Given the voltage pictures in the eight operating phases, as illustrated in Fig. 3(a), the relation among the intermediate voltages V_0 to V_3 and the storage voltage V_b are formulated as follows

$$\begin{bmatrix} 1 & 0 & 0 & 1\\ \gamma_1 & -1 & 0 & 0\\ 0 & \gamma_2 & -1 & 0\\ 0 & 0 & \gamma_3 & -1 \end{bmatrix} \begin{bmatrix} V_0\\ V_1\\ V_2\\ V_3 \end{bmatrix} = \begin{bmatrix} 2V_{oc}\\ (\gamma_1 - 1)(V_b + V_d)\\ (\gamma_2 - 1)V_d\\ (\gamma_3 - 1)(-V_b + V_d) \end{bmatrix}$$
(1)

where $V_{oc} = I_0/(\omega C_p)$ is the nominal open-circuit voltage, I_0 is the magnitude of i_{eq} ; ω is the vibration frequency; γ_1 , γ_2 , and γ_3 are the *flipping factor* in each bias-flip action (phase 2, 3, and 4). They are defined as the voltage change ratios after the bias-flip actions (the bias voltage is regarded as the referenced neutral level for the voltage flipping). Since all the three bias-flip transients in each synchronized instant share the same r- L_i - C_p circuit branch, $\gamma_1, \gamma_2, \gamma_3$ equal to the same number $\gamma = -e^{-\pi/(2Q)}$ if all bias-flip actions are activated. On the other hand, some of the bias-flip actions might be deactivated under the charging-start period or small load resistance, given their attempts to reversely conduct the corresponding current steering diode. Such automatic deactivation is of importance for realizing the self-startup and selfadaptive features of the SMBF designs [10]. When a specific bias-flip action is deactivated because of the unidirectional diode, v_p keeps still, the corresponding flapping factor should be just unity, i.e., $\gamma_x = 1$ (x = 1, 2, or 3).

According to (1), the intermediate voltages in the downstairs bias-flip actions, i.e., V_0 , V_1 , V_2 and V_3 , can be expressed as functions of V_{oc} , V_b , and V_d . The transient behavior of the S-S3BF circuit is similar to that in its P-S3BF counterpart [10]. The storage capacitor C_b is gradually charged up towards the steady state. During the transient, the bias voltage V_b also gradually increase from zero by going through three transient stages from single, to double, and to triple bias-flip operations. The three transient stages, the corresponding valid bias-flip



Fig. 5. The steady-state piezoelectric voltage v_p (red) and bias/storage voltage v_b (blue) under the (a) heavy load, (b) medium load, and (c) light load.

actions, and the equivalent flipping factors in each stage are listed in Table I.

The same equation can be utilized to derive the intermediate voltages under different stages by replacing the three sets of flipping factors. The two critical bias/storage voltages connecting the single-, double-, and triple-BF stages can be solved as follows

$$V_{b,C1} = -\gamma (V_{oc} - V_d) \tag{2}$$

$$V_{b,C2} = \frac{2\gamma}{\gamma^2 - 1} (V_{oc} - V_d)$$
(3)

When $V_b < V_{b,C1}$, only the 1^{st} bias-flip action is activated. The system runs at the single bias-flip stage, which is equivalent to S-S1BF or S-SSHI. when $V_{b,C1} < V_b < V_{b,C2}$, the 1^{st} and 3^{rd} actions are activated. The system runs at double biasflip stage, which is equivalent to S-S2BF. When $V_b > V_{b,C2}$, all of the three bias-flip actions are activated. The system runs at the triple bias-flip stage; the S3BF operation is finally obtained.

TABLE II Parameters in Experiment.



Fig. 6. The harvested power under different bias/storage voltages.

The triple bias-flip operation is not necessarily attainable. Under heavily loading condition, i.e., small R_l , more power from C_b is consumed during the open circuit phases. Therefore, V_b might hardly rise to $V_{b,C1}$ and steadily stay at the S1BF zone, as shown by the blue charging curve in Fig. 4. Under medium and light load, V_b might enter and stay at the S2BF and S3BF zones, respectively.

IV. RESULTS

Experiments are carried out to validate the design. The mechanical and electrical parameters are listed in Table II. The experimental waveforms under heavy (16 k Ω), medium (49 k Ω), and light load (480 k Ω) conditions are shown in Fig. 5. The observation agrees with the analysis, the bias/storage voltage v_b steadily stays in the three zones under the three loading conditions, respectively.

To quantitatively evaluate the harvested power, the equivalent impedance modeling technique [4], [15] is adopted for formulating the dynamics under different V_b . Since the similar formula was also used in the P-S3BF analysis [10], it is not repeated here. Fig. 6 shows the harvested power under different bias/storage voltage V_b . It illustrates how does the harvested power automatically shift from S1BF, S2BF, to S3BF operations by following the envelope curves.

V. CONCLUSION

The piezoelectric energy harvesting (PEH) capability can be enhanced by simultaneously increasing the piezoelectric voltage magnitude and decreasing the pace of voltage jumps at every synchronized instant. This paper has proposed the series synchronized triple bias-flip (S-S3BF) interface circuit for PEH enhancement. Compared to the existing topology, the S-S3BF use only one external capacitive component to realize the energy storage and triple bias-flip function, which makes the best use of the passive components. The operation and automatically shifting features were analyzed in details. Experimental results have validated the analysis and demonstrated the effectiveness of S-S3BF.

REFERENCES

- G. D. Szarka, B. H. Stark, and S. G. Burrow, "Review of power conditioning for kinetic energy harvesting systems," *IEEE Transactions* on *Power Electronics*, vol. 27, no. 2, pp. 803–815, Feb 2012.
- [2] M. Y. Benslimane, H.-E. Kiil, and M. J. Tryson, "Dielectric electroactive polymer push actuators: performance and challenges," *Polymer International*, vol. 59, no. 3, pp. 415–421, 2010.
- [3] A. Hajati and S.-G. Kim, "Ultra-wide bandwidth piezoelectric energy harvesting," *Applied Physics Letters*, vol. 99, no. 8, p. 083105, 2011.
- [4] J. Liang and W.-H. Liao, "Impedance modeling and analysis for piezoelectric energy harvesting systems," *IEEE/ASME Transactions on Mechatronics*, vol. 17, no. 6, pp. 1145–1157, 2012.
- [5] Y. Liu, G. Tian, Y. Wang, J. Lin, Q. Zhang, and H. F. Hofmann, "Active piezoelectric energy harvesting: General principle and experimental demonstration," *J. Intell. Mater. Syst. Struct.*, vol. 20, no. 5, pp. 575–585, Mar. 2009.
- [6] D. Kwon and G. A. Rincón-Mora, "A Single-Inductor 0.35 μm CMOS Energy-Investing piezoelectric harvester," *IEEE J. Solid-State Circuits*, vol. 49, no. 10, pp. 2277–2291, Oct. 2014.
- [7] M. Lallart and D. Guyomar, "Piezoelectric conversion and energy harvesting enhancement by initial energy injection," *Appl. Phys. Lett.*, vol. 97, no. 1, p. 014104, Jul. 2010.
- [8] J. Dicken, P. D. Mitcheson, I. Stoianov, and E. M. Yeatman, "Power-Extraction circuits for piezoelectric energy harvesters in miniature and Low-Power applications," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4514–4529, Nov. 2012.
- [9] J. Liang, "Synchronized bias-flip interface circuits for piezoelectric energy harvesting enhancement: A general model and prospects," *Journal* of Intelligent Material Systems and Structures, vol. 28, no. 3, pp. 339– 356, 2017.
- [10] J. Liang, Y. Zhao, and K. Zhao, "Synchronized triple Bias-Flip interface circuit for piezoelectric energy harvesting enhancement," *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 275–286, Jan. 2019.
- K. Zhao, J. Liang, and C. Chen, "Parallel synchronized septuple bias-flip circuit for piezoelectric energy harvesting enhancement," in *IECON 2017* - 43rd Annual Conference of the IEEE Industrial Electronics Society, Oct 2017, pp. 2629–2634.
- [12] P. Gasnier, J. Willemin, S. Boisseau, G. Despesse, C. Condemine, G. Gouvernet, and J.-J. Chaillout, "An autonomous piezoelectric energy harvesting ic based on a synchronous multi-shot technique," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 7, pp. 1561–1570, 2014.
- [13] Z. Chen, M. K. Law, P. I. Mak, W. H. Ki, and R. P. Martins, "22.2 a 1.7mm2 inductorless fully integrated flipping-capacitor rectifier (fcr) for piezoelectric energy harvesting with 4832017 IEEE International Solid-State Circuits Conference (ISSCC), Feb 2017, pp. 372–373.
- [14] S. Du and A. A. Seshia, "An inductorless bias-flip retifier for piezoelectric energy harvesting," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 10, pp. 2746–2757, Oct 2017.
- [15] J. Liang, H. S.-H. Chung, and W.-H. Liao, "Dielectric loss against piezoelectric power harvesting," *Smart Materials and Structures*, vol. 23, no. 9, p. 092001, 2014.