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A Cross Regulation Reduced Multi-Output and Multi-VCR Piezoelectric Energy Harvesting System Using Shared Capacitors

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***Abstract*—This paper presents a triple-output piezoelectric energy harvesting (PEH) system with parallel synchronized switch harvesting on capacitors (P-SSHC) rectifier based on shared capacitors. By analyzing the principle of the P-SSHC rectifier, this paper supports the rationality of using shared capacitors to construct the multi-voltage conversion ratio (VCR) switch capacitor (SC) DC-DC converters. In addition, the adoption of a parallel structure in the multi-output SC DC-DC converters reduces the cross-regulation. Simulation results show that the proposed system not only has good input power adaptability (1/3X,1X,2X) but can also provide triple voltage (0.5V, 1V, 2V) with less cross-regulation. The maximum output power is 14.4μW when peak-to-peak open circuit voltage is 1.7V.**

***Index Terms*—Piezoelectric energy harvesting, parallel synchronized switch harvesting on capacitors, shared capacitors.**

I. Introduction

With the rapid development of the Internet-of-Things (IoT), wireless sensor networks (WSN) have drawn significant interest given their ability to better connect people with the physical world around them. However, due to their large size and limited lifetime, traditional batteries are not suitable for the wireless sensor nodes [1]. Piezoelectric energy harvesting (PEH) is one possible way for these applications by converting vibration mechanical energy into the electrical energy. In order to provide a stable dc to the load, the interface circuits of PEH are necessary. Several inductor-based techniques, such as synchronous electric charge extraction (SECE) [2] and parallel synchronized switch harvesting on inductor (P-SSHI) [3] have been proposed. By using the principle of LC resonance, the inductor-based techniques can recycle the charge on C_p and thus achieve high energy extraction efficiency. However, the large off-chip high-Q inductors required make the inductor-based techniques unattractive for full integration.

Recently, the capacitor-based techniques, including parallel synchronized switch harvesting on capacitors (P-SSHC), the flipping-capacitor rectifier (FCR), split-phase flipping-capacitor rectifier (SPFCR), multilevel synchronized switch harvesting on capacitors (ML-SSHC) [4-8], have been proposed to recycle the energy from C_p by capacitors. These techniques all retain advantages of small size and easy integration. Among these techniques, the P-SSHC rectifier is

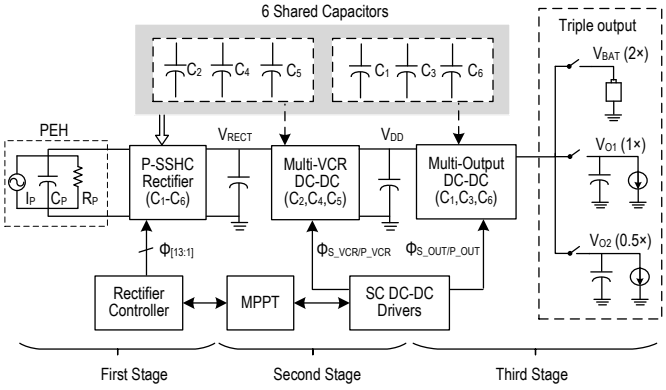


Fig. 1. System architecture of the proposed system

especially attractive because of its simple structure and stable performance. However, up to this point, the capacitor-based techniques have been limited to providing a single fixed output voltage. Some applications for IoT require multiple voltage levels to power different blocks of the device [9-11]. In multi-output converters, each output is expected to adjust independently; cross-regulation occurs if the output voltage of one converter is affected by the load change of the other converter. In a worst case scenario, the entire converter may become unstable.

To fill in gaps that currently exist in previous research, this paper proposes a triple-output piezoelectric energy harvesting system with the P-SSHC rectifier based on shared capacitors. By sharing six capacitors among the P-SSHC rectifier, multi-VCR SC DC-DC converters, and multi-output SC DC-DC converters, the proposed system avoids the use of passive devices that require additional cost and volume, and thus enhancing the capacitor utilization and system compactness. Moreover, this paper further analyzes the principle of the P-SSHC rectifier based on the work of Chen et al [7] and applies this principle to the proposed multi-VCR SC DC-DC converters, allowing the system to maintain high energy efficiency over a wide range of input power. Furthermore, by using a parallel structure to construct the multi-output SC DC-DC converters, we effectively reduced cross regulation under load-step transient.

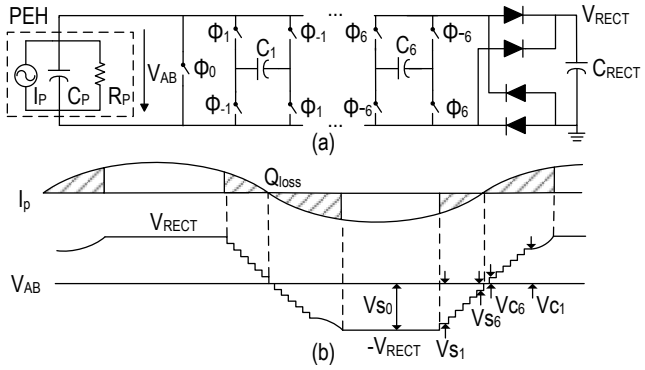


Fig. 2. P-SSHC rectifier with 6 SCs and associated waveforms

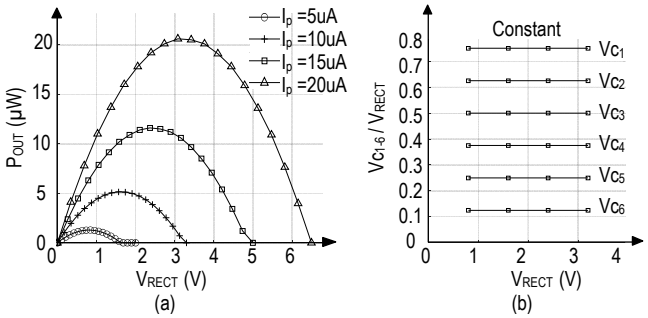


Fig. 3. (a) Simulated P_{OUT} with respect to V_{RECT} at different excitation. (b) Ratios of voltages on flying capacitors Vc_i over rectifier voltage V_{RECT}.

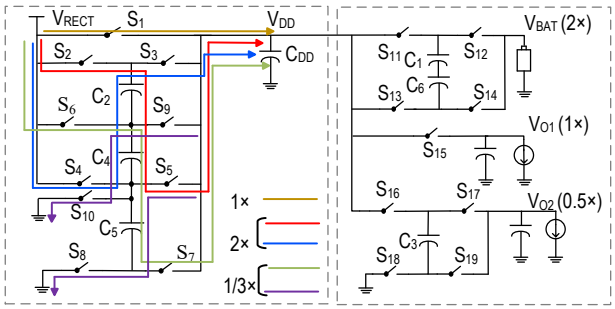
II. Proposed Multi-output PEH System

A. System Architecture

The system architecture of the proposed system is shown in Fig. 1. The whole system consists of three stages: the first stage consists of P-SSHC rectifier based on six capacitors. The second stage includes the multi-VCR SC DC-DC converters which are designed to regulate the output voltage of the rectifier V_{RECT} under the control of the maximum power point tracking (MPPT) module. The system can thus maintain high energy efficiency over a wide range of input power. The third stage consists of the multi-output SC DC-DC converters. Through two independent SC DC-DC converters, V_{DD} is converted to three stable regulated dc output voltages: V_{BAT}, V_{o1}, and V_{o2}. It is worth noting that the first, second, and third stage of the system share six flying capacitors. Specifically, P-SSHC rectifier uses six flying capacitors, $C_1 - C_6$, to flip the voltage across C_p during the flipping time, i.e., the zero-crossing moment of I_P. During non-flipping time, flying capacitors C_2, C_4, and C_5 are used to construct the multi-VCR DC-DC converters, while flying capacitors C_1, C_3, and C_6 are used to construct the multi-output DC-DC converters.

B. Analysis of P-SSHC Rectifier

Fig. 2 shows P-SSHC rectifier with 6 SCs and the associated waveforms [5]. At each zero-crossing moment of I_P, 25 analog switches are driven by 13 pulse signals to flip the voltage across C_p. The 13 non-overlapping switching signals are generated and then sequenced depending on the flip



Multi-VCR DC-DC Converter

VCR	Cap	Switch On
1	No	S_1
2	C_2 C_4	Φ_S : S_2, S_5 Φ_P : S_3, S_4
1/3	C_4 C_5	Φ_S : S_6, S_7 Φ_P : S_5, S_8, S_9,S_{10}

Multi-output DC-DC Converter

VCR	Cap	Switch On
1	No	S_{15}
2	C_1 C_6	Φ_S : S_{11}, S_{14} Φ_P : S_{12}, S_{13}
1/2	C_3	Φ_S : S_{16}, S_{19} Φ_P : S_{17}, S_{18}

Fig. 4. Circuit of SC DC-DC converters

direction of V_{AB}. To flip V_{AB} from $-V_{RECT}$ to V_{RECT}, the phase order of the 13 pulses is ϕ_1, ..., ϕ_6, ϕ_0, ϕ_{-6}, ..., ϕ_{-1}. Alternatively, when V_{AB} is flipped from V_{RECT} to $-V_{RECT}$, the phase sequence is reversed. Due to symmetrical operations, the principle of P-SSHC rectifier was analyzed from negative to positive. In order to balance the voltage flip efficiency and stability time, flip capacitors were sized as $C_1 = ... = C_6 = C_p$ [12]. The analysis is based on the premise that the whole circuit is under steady state. Vs_i and $Vc_i(i = 1 - 6)$ are assumed to be the shared voltage and rebuilt voltage of flying capacitor $C_i(i = 1 - 6)$, respectively. According to the law of charge conservation, we obtain

$$\phi_i : C_p Vs_{i-1} + C_i Vc_i = (C_p + C_i) Vs_i \tag{1}$$

$$\phi_{-i} : C_p Vc_{i+1} + C_i Vs_i = (C_p + C_i) Vc_i \tag{2}$$

where $Vs_0 = V_{RECT}$, $Vc_7 = 0$. Adding (1) and (2) leads to

$$Vc_1 + Vs_1 = V_{RECT} \tag{3}$$

Since $C_i = C_p$, we can get

$$Vs_i = (8 - i) Vc_6 \tag{4}$$

Equations (1)-(4) above can be solved simultaneously

$$Vc_i = \frac{7 - i}{8} V_{RECT} \tag{5}$$

Theoretically, the voltage-flipping efficiency of the P-SSHC rectifier

$$\eta = \frac{Vc_1 + V_{RECT}}{2V_{RECT}} = 0.875 \tag{6}$$

where V_{RECT} is the output voltage of the rectifier. As can be seen above in (5), the ratios of Vc_1-Vc_6 over V_{RECT} are constant, which can be calculated as 0.75, 0.625, 0.5, 0.375, 0.25, and 0.125, respectively.

Fig. 3 (a) shows the simulated P_{out} at different excitation I_p. As I_p increases, the corresponding rectifier output V_{RECT} of the maximum output power obtained by PEH system increases

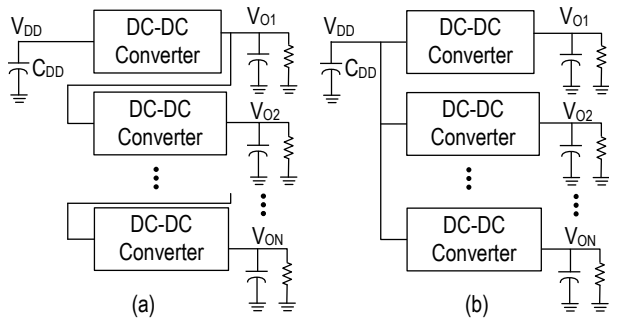


Fig. 5. Two structures of multi-output DC-DC converters. (a) Series structure. (b) Parallel structure.

TABLE I
CAPACITOR COMBINATIONS OF DC-DC CONVERTERS

Conversion Rate	Combination	Voltage Mismatch ΔV
0.5	$\boldsymbol{C_3}$	$\mathbf{0}$
	C_4 , C_6	0
2	C_1 , C_4	$0.125V_{RECT}$
	C_1 , C_5	0
	C_1 , C_6	$0.125V_{RECT}$
	$\boldsymbol{C_2}$, $\boldsymbol{C_3}$	$\boldsymbol{0.125V_{RECT}}$
	$\boldsymbol{C_2}$, $\boldsymbol{C_4}$	$\mathbf{0}$
1/3	$\boldsymbol{C_4}$, $\boldsymbol{C_5}$	$\boldsymbol{0.125V_{RECT}}$
	C_4 , C_5 , C_6	$0.083V_{RECT}$

Note: This table lists only $\Delta V <$ 0.13 V_{RECT}

accordingly. Therefore, in order to achieve maximum power output under different excitation I_p, the PEH system needs multi-VCR DC-DC converters to achieve maximum power point tracking. Fig. 3 (b) illustrates that when the excitation varies, the ratios of voltages on flying capacitors Vc_i over rectifier voltage V_{RECT} are constant. This is consistent with the above calculation results, thus providing a theoretical basis for constructing multi-VCR DC-DC converter using shared capacitors.

C. SC DC-DC Converters

Fig. 4 shows the circuit of SC DC-DC converters, which can be divided into two parts: multi-VCR and multi-output DC-DC converters. The multi-VCR DC-DC converters are constituted by flying capacitors C_2, C_4, and C_5. Specifically, C_2 and C_4 are used in series at VCR=2 while C_4 and C_5 are used at VCR=1/3. Here, C_4 is shared in both VCRs. At VCR=1, S_1 bypasses all capacitors and V_{RECT} is directly connected to V_{DD}. The multi-output DC-DC converters are constituted by flying capacitors C_1, C_3, and C_6. Specifically, C_1 and C_6 are utilized to generate 2× output voltage to charge battery V_{BAT} and C_3 are used to generate 0.5× output voltage to supply digital load V_{o2}; Simultaneously, analog load is powered by 1× output voltage using S_{15}. There are two main considerations when constructing the converters.

Consideration 1: Capacitor combinations with less voltage mismatch should be selected to minimize the charge distribution loss. Table I lists some possible capacitor combinations and their corresponding voltage mismatches. The voltage mismatch refers to the difference between the voltage of the flying capacitors and the voltage of the DC-DC converters. Small voltage mismatch reduces the charge redistribution loss in the conversion process, and hence the system can achieve high efficiency. In order to minimize the sum of voltage mismatches, we use the highlighted capacitor combination as shown in the table. Note that the possible combinations are more than that. If necessary, these six capacitors can be utilized to implement more conversion ratios and output voltages.

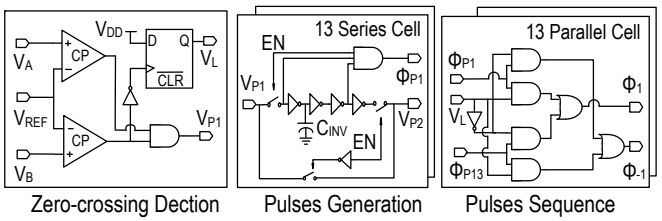


Fig. 6. Controller circuit of P-SSHC rectifier

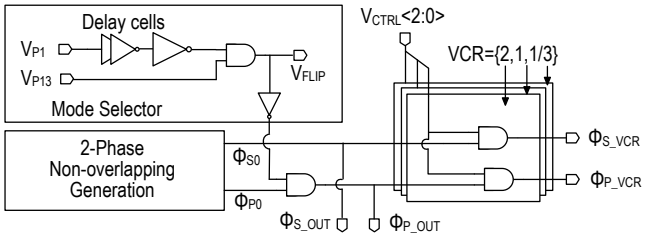


Fig. 7. The circuit of SC DC-DC drivers

Consideration 2: A parallel structure should be used to construct multi-output DC-DC converters. Generally, multi-output DC-DC converters can adopt series and parallel circuit structures. As shown in Fig. 5(a), output voltages can be generated by connecting several DC-DC converters in series and deriving the internal nodes of the converters. However, due to the interaction between internal nodes, this type of configuration usually has a serious cross-regulation problem. Fig. 5(b) shows the proposed structure, in which several independent DC-DC converters are connected in parallel to provide different outputs. Since each independent DC-DC converter only affects the node voltage V_{DD}, and the capacitance of C_{DD} is large, the influence of cross-regulation between different outputs is greatly reduced.

III. KEY BUILDING BLOCKS

A. Rectifier Controller

The design of controller circuit of P-SSHC rectifier is similar to that as proposed by [5]. Its structure is shown in Fig. 6 and is composed of zero-crossing detection, pulses generating, and pulses sequencing. When I_P is close to zero, the diodes of FBR are on the verge of turning off. At this moment, one of either V_A or V_B is close to $V_{RECT} + V_D$ while the other one is close to $-V_D$. Therefore, by using two continuous time comparators to compare V_A, V_B and reference voltage V_{REF}, zero-crossing detection can obtain signal V_{P1}, whose rising edge represents the moment of I_p zero-crossing. Following the rising edge of V_{P1}, 13 pulses are sequentially generated by a pulse generation module while a

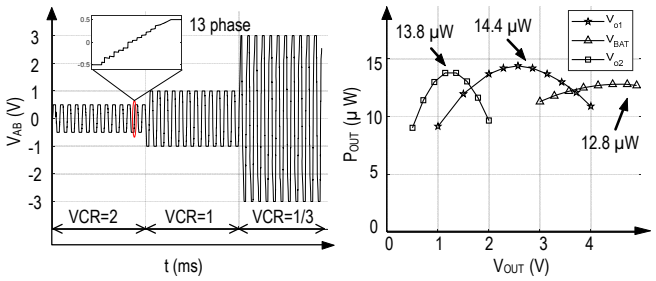


Fig. 8. (a) Simulated V_{AB} with 13-phase P-SSHC under MPPT (b) Simulated P_{OUT} at different outputs.

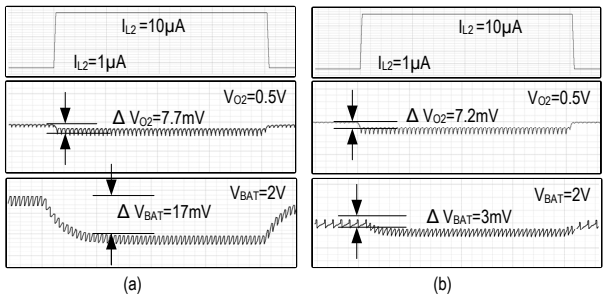


Fig. 9. Cross regulation of multi-output SC DC-DC converters with series and parallel structures. (a) Series structure (b) Parallel structure

pulse sequencing module is also implemented to reorder those signals.

B. SC DC-DC Drivers

The SC DC-DC drivers are shown in Fig. 7. Since the P-SSHC rectifier, multi-VCR DC-DC converters, and multi-output DC-DC converters share six flying capacitors, additional mode selector is necessary to avoid capacitor access conflicts. The rising edge of V_{P1} and V_{P13} represents the generation of the first and last pulse signals, respectively. By ANDing the two signals with inverters and delay cells, the signal V_{FLIP} can be obtained and used to determine the amount of time the flying capacitors were used by P-SSHC rectifier. Two phase non-overlapping pulse signals, Φ_{S0}, Φ_{P0}, and V_{FLIP} are processed to obtain the driver signals of the multi-output DC-DC converters. Φ_{SOUT}, Φ_{POUT}, together with $V_{CTRL<2:0>}$ as provided by the MPPT module are processed to generate the driving signals of multi-VCR DC-DC converters.

IV. Simulation Results

The simulation parameters were set as follows: an inherent capacitance C_p = 15nF, inherent resistance R_p = 10MΩ, current source frequency f_p = 250Hz, and flying capacitors C_1 = ... = C_6 = 15nF. When I_p varies, the MPPT module can maintain a maximum output power by regulating V_{RECT}, the multi-VCR DC-DC converters then converting V_{RECT} to a fixed output voltage of 1V. Fig. 8 (a) shows the waveform of P-SSHC rectifier under MPPT control. When the VCR is 2, 1 and 1/3, the voltage flipping efficiencies are approximately 0.865, 0.894 and 0.856. Compared with the theoretical voltage-flipping efficiency of 0.875, the efficiencies are slightly different under varying VCR. This is caused by the fact that the initial voltages of flying capacitors are not zero under different excitation but progressively accumulate to a certain extent. Fig. 8 (b) shows the output power with respect to different V_{OUT} when peak-to-peak open circuit voltage V_{PP}=1.7V. V_{o1} has the highest output power, around 14.4μW. This is because V_{o1} is directly connected to V_{DD} without going through multi-output DC-DC converters, thus saving substantial switching loss. The maximum output power of V_{o2} is higher than that of V_{BAT} because less voltage mismatch results in less energy loss.

TABLE II
Comparison with State-of-the-Art Works

	This Work	18'ISSCC[6]	19'ISSCC[7]	20'JSSC[8]
Verification	Simulation	Measurement	Measurement	Measurement
Technology	0.18μm	0.18μm	0.18μm	0.18μm
Rectifier	P-SSHC	SE-SSHC	SPFCR	ML-SSHC
C_p	15nF	1.94pF	22nF	6nF
Frequency	250Hz	219Hz	200Hz	22Hz
Key Components	6 capacitors 13 phase 90nF	8 capacitors 17 phase 4nF	4 capacitors 21 phase 272nF	4 capacitors 7 phase 600pF
Output voltage	3	1	1	1
P_{in} adaption	Yes	No	Yes	No
Max efficiency	0.894	0.69	0.84	0.75

Fig. 9 shows the cross-regulation phenomena of multi-output SC DC-DC converters with series and parallel structures. When the load current of V_{o2} suddenly changes from 1μA to 10μA while the load current of V_{o1} is 0, the series structure will let the V_{o2} and V_{BAT} decreased by about 7.7mV and 17mV, respectively. However, by using the proposed parallel structure to construct the multi-output SC DC-DC converter, V_{BAT} decreased only by 3mV when V_{o2} at the output decreased by 7.2mV, thus effectively reducing the cross-regulation problem. Table II shows the performance summary and benchmark with the other PEH systems.

V. Conclusion

This paper presents a multi-output and multi-VCR piezoelectric energy harvesting system using shared capacitors. By analyzing the working principle of the P-SSHC rectifier, this paper demonstrates the rationality of using shared capacitor to construct multi-VCR SC DC-DC converter. The simulation results show that the system is able to generate triple output voltages of 0.5V, 1V ,and 2V for external load and cross-regulation of the multi-output converters is minimized by using a parallel structure.

Acknowledgement

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