

A Synchronized Multiple Bias-flip Interface Circuit for Piezoelectric Energy Harvesting Using Optimized Switched-Capacitor Arrays

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Abstract—This paper introduces a new implementation of the synchronized multiple bias-flip (SMBF) interface circuit for piezoelectric energy harvesting systems. The proposed circuit uses an optimized and easy-to-drive capacitor array for multiple voltage bias-flip actions. The switched-capacitor array consists of five capacitors. It is able to carry out 27 continuous voltage bias-flip actions by re-organizing the multiple capacitors and properly reusing them in different phases. The proposed circuit topology extracts more power than the previously proposed harvesting circuit, which again validates the optimal SMBF theorem. It also explores the potential and reveals the limitations of piezoelectric energy harvesting improvement by using multiple bias-flip actions.

Index Terms—Energy harvesting, piezoelectric, synchronized switch interface circuit

I. INTRODUCTION

Apart from the electric energy supplied by the artificial power grid, different forms of energy are widely available in the ambient environment. By exploiting and properly utilizing these ambient energy sources, future distributed electronic devices can become battery-free. In this way, the maintenance cost of the ubiquitous Internet of Things (IoT) network can be greatly reduced. Among all the ambient energy sources, kinetic energy has been extensively studied to power the IoT or wearable devices where motion energy is abundant in the surroundings.

Piezoelectric transducers (PT) are suitable for kinetic energy harvesting due to their simple configuration (compared with electromagnetic energy harvesters) and relatively high electromechanical coupling coefficient (compared with electrostatic energy harvesters). Interface circuits are needed to convert the alternating output voltage from a PT into a regulated dc voltage for powering digital electronics. A full-bridge rectifier (FBR), which is also called standard energy harvesting (SEH), is a typical and the easiest interface circuit for piezoelectric energy harvesting (PEH). It is regarded as the benchmark in many papers for evaluating the performances of PEH interface circuits [1], [2].

The output impedance of PT is capacitive. The capacitance is usually around pF to nF level and the vibration frequency is usually below 1 kHz; therefore, the output impedance of a PT is relatively large. In order to passively compensate for

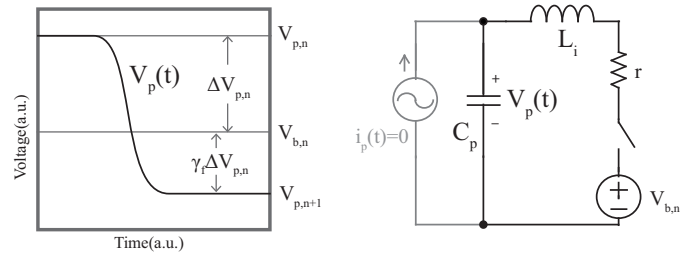


Fig. 1. Generalized equivalent circuit (right) and voltage waveform (left) in a voltage bias-flip action. For conventional SECE, bias voltage $V_{b,n} = 0$; inversion factor $\gamma = 0$. For conventional SSHI, $V_{b,n} = 0$.

this output impedance, we need to connect an inductive load with tens or even hundreds of henry. Such an inductor is huge in size. It is impractical to follow such a linear compensation system to realize maximum power extraction.

The synchronized switch technique, called synchronous electric charge extraction (SECE), was proposed in about 2005 [3]. A switched inductor is connected to shunt the piezoelectric capacitance in a transient to extract the stored energy in the PT at every synchronized instant. Such an extraction rapidly resets the voltage across a PT to zero. Resetting the transducer voltage in the right instants helps improve the conduction angle of the bridge rectifier. Besides SECE, another solution called parallel synchronized switch harvesting on inductor (P-SSHI) further flips the transducer voltage to its opposite sign direction [4]. The greater the extent of the voltage bias flip, the better its harvesting performance will be. The ability of voltage flipping is defined by a flipping factor γ . The flipping factor γ is formulated by

$$V_{p,n+1} = -\gamma V_{p,n}, \quad \gamma \in (-1, 0], \quad (1)$$

where $V_{p,n+1}$ and $V_{p,n}$ are the piezoelectric voltage before and after a bias-flip action. Fig. 1 shows the equivalent circuit and voltage waveform of a bias-flip action. After the synchronized switch technique has been proposed, many other energy harvesting interface circuits based on the synchronized switch principles have been proposed, such as the series SSHI (S-SSHI) [1] and the synchronous inversion and charge extraction (SICE) [2].

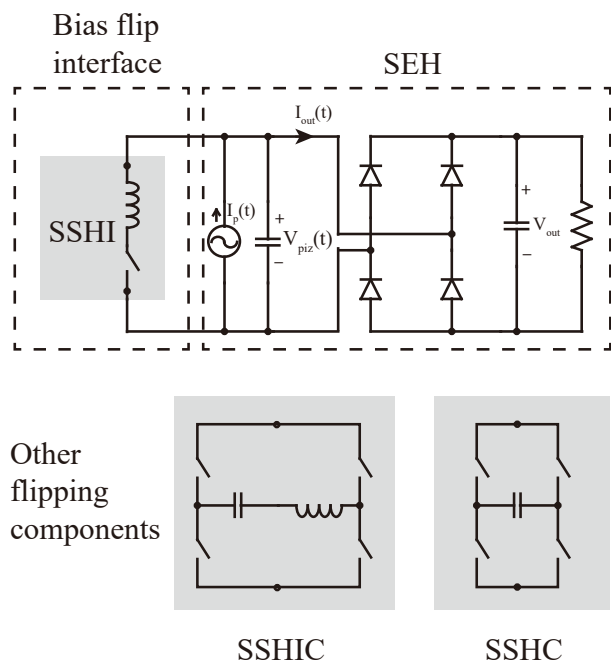


Fig. 2. Circuit Topologies of SSHI, SSHIC, and SSHC.

In P-SSHI, the voltage is flipped through an inductor. Besides that, other components can also be added in the bias-flip circuit branch to construct different designs, as shown in Fig. 2. To achieve an inductor-less design, the synchronized switch harvesting on capacitor (SSHC) was proposed [5]. A large storage capacitor shunts the PT forwardly and reversely to perform charge exchange and flip the transducer voltage. Ref. [6] uses multiple capacitors to form a switched-capacitor array and breaks the flipping process into multiple steps. Such a design reduces the energy dissipation during the voltage flipping actions. Another flipping component is a series circuit of an inductor and a capacitor. In the flipping process, a C-L-C resonant circuit loop is formed to flip the voltage across the PT. In this configuration, the need for a high-quality factor inductor is greatly relieved [7]. The C-L-C resonant loop has also been applied to multiple bias-flip circuits. Ref. [8] reported a 13 bias-flip harvesting circuit using six capacitors and an inductor. It proved that, under the same capacitor array configuration, the C-L-C resonant loop performs better than the C-C charge exchange scheme used in the SSHC circuits.

In [9], a general mathematical model of synchronized multiple bias flip (SMBF) is developed. SMBF theory suggests that multiple voltage flipping results in better γ , thus a superior harvesting performance [9]. Multiple LC resonances with respect to different dc bias voltages help rapidly change the transducer voltage more flexibly. Based on the SMBF model, more practical implementations were proposed, such as P-S3BF [10], P-S7BF [11], S-S3BF [12]. In these works, different capacitor arrays are recombined with a switch network forming a series of dc bias voltages.

In this paper, a new PEH circuit, which is developed

based on the SMBF model, is introduced. A voltage bias-flip interface using a low-profile inductor and a capacitor array is designed to improve the energy harvesting capability. The capacitor array is optimally selected to achieve as many bias-flip actions as possible in each synchronized switch instant while maintaining the easy-to-drive nature as the previous SMBF-based interface circuits. A prototype circuit is implemented with discrete components to operate under a high piezoelectric voltage.

II. OPTIMAL DESIGN OF BIAS CAPACITOR ARRAY

The design goal is to generate as many stable voltage levels as possible as bias sources by reconstructing a given number of capacitors using series or parallel connections. According to the SMBF theorem, the capacitor array needs to produce some evenly distributed voltages, which are asymmetric with respect to zero in the parallel-SMBF case, to achieve maximum harvested power output. Considering this design target and constraints, the capacitor array is optimally designed by going through all possible combinations. Such a brutal-force search might be facilitated with some proper numerical solution in the future.

Fig. 3 shows the circuit topology of the proposed SMBF implementations, when using one capacitor (forming the maximum triple bias-flip case) to five capacitors (forming the maximum 27 bias-flip case). It is a parallel-type SMBF harvesting circuit, which consists of a shunt bridge rectifier branch and a voltage bias-flip branch. The voltage bias-flip branch is formed by an inductor and a capacitor array. Four MOSFETs and two diodes are used in each current steering network unit, which is represented by a red diamond in the figure. A PMOS S_{N1} and an NMOS S_{N2} form a bidirectional switch. An NMOS S_{N3} with one current-steering diode and a PMOS S_{N4} with another current-steering diode form two paths for current direction control. Each node of the capacitor array V_{CN} can be connected to V_{b+} or V_{b-} according to the switch commands from the controller. The source terminals of S_{N2} , S_{N3} and S_{N4} are connected to a steady voltage V_{CN} , while that of S_{N1} is connected to V_{CN} via the body diode of S_{N2} . So all four transistors in a switch unit can be driven with simple RC bootstrap networks.

III. OPERATION PRINCIPLE

The circuit operates by connecting the bias capacitor banks in different combinations to achieve multiple voltage bias-flip actions. With the help of the current steering network, the piezoelectric capacitance and flipping inductor L can form an LC resonant network while the capacitor array provides different dc bias voltages.

Table I shows the control sequences of all these five topologies with one to five bias capacitors, respectively. After the optimal configuration, the possible constructed bias voltage levels V_{Gn} and the utilized current-steering units are also listed in the table. The connected voltage level and default current

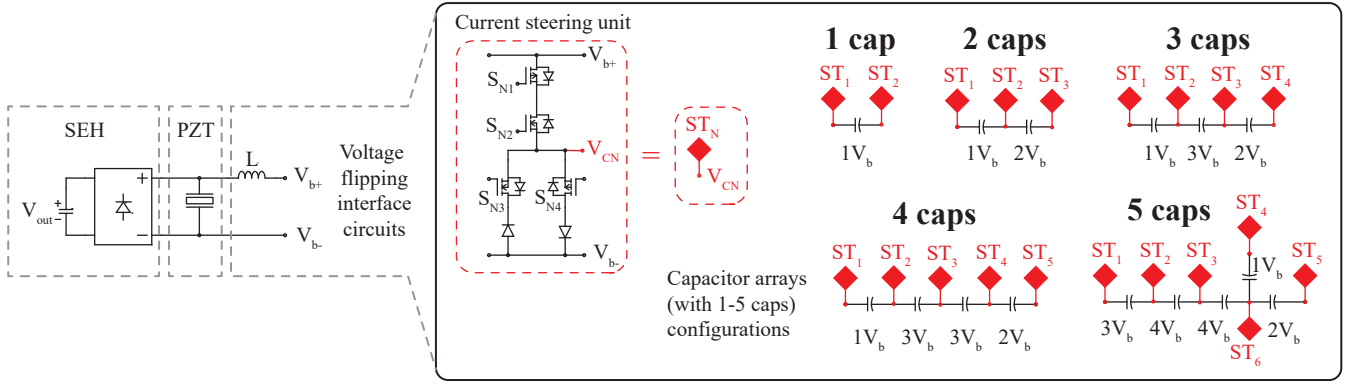


Fig. 3. Optimized capacitor array configurations and circuit topology of the proposed implementation of SMBF circuit, from using one to five capacitors, respectively.

TABLE I
GENERATED BIAS VOLTAGE AND CORRESPONDING SWITCH-ON UNITS.

$\pm V_{Cn}$	1 Cap	2 Caps	3 Caps	4 Caps	5 Caps
0	ST1, ST1	ST1, ST1	ST1, ST1	ST1, ST1	ST1, ST1
$1V_b$	ST1, ST2	ST1, ST2	ST1, ST2	ST1, ST2	ST4, ST6
$2V_b$	-	ST2, ST3	ST3, ST4	ST4, ST5	ST5, ST6
$3V_b$	-	ST1, ST3	ST2, ST3	ST2, ST3	ST1, ST2
$4V_b$	-	-	ST1, ST3	ST1, ST3	ST2, ST3
$5V_b$	-	-	ST2, ST4	ST3, ST5	ST3, ST4
$6V_b$	-	-	ST1, ST4	ST2, ST4	ST3, ST5
$7V_b$	-	-	-	ST1, ST4	ST1, ST3
$8V_b$	-	-	-	ST2, ST5	ST2, ST6
$9V_b$	-	-	-	ST1, ST5	ST2, ST4
$10V_b$	-	-	-	-	ST2, ST5
$11V_b$	-	-	-	-	ST1, ST6
$12V_b$	-	-	-	-	ST1, ST4
$13V_b$	-	-	-	-	ST1, ST5

direction in each phase can be set by a digital controller according to the designated control rules.

Taking the three capacitor banks case, for example, the working principle is demonstrated in Fig. 4. Using three capacitors can furthest realize 13 bias-flip actions in each synchronized instant under steady-state. The waveform on the right is $V_{pz}(t)$ in the downstairs (from positive to negative) voltage flipping action. Fig. 4 only shows downstairs operation because the operation modes of upstairs voltage flipping are symmetric using the complementary switching branches. For other capacitor arrays, the working principle is similar, the only difference is how many capacitors are involved in the voltage-flipping process.

For a more concise expression, the MOSFETs are illustrated with ideal switches. The voltage of the output terminal V_{out} is constant under steady state. All components are considered ideal in this study, except for the inductor with a limited quality factor. The voltages on bias capacitors are regarded as stable constants.

1) *Energy output phase*: Before the zero crossing point of i_p , the circuit works in the shunt charging condition, as shown in Fig. 4(a). i_p is delivered to the storage or load through the diode bridge. The voltage-flipping interface is inactive in this

phase. This phase processes until $i_p(t)$ drops and crosses zero.

2) *Bias-flip phases*: At the beginning of the voltage-flipping action, the diode bridge is blocked since $|V_{pz}| < V_{out}$. The current steering network steers the current to the capacitor array. C_p , L , and capacitor array form a biased LC resonant circuit. Since C_p is relatively small, the resonant frequency of this LC circuit is usually at a few thousand Hz, which is much higher than the resonant frequency of typical cantilever beams. Therefore, during the voltage-flipping action, as illustrated in Fig. 4(b)–(n), i_p can be regarded as zero.

In the sub-phase shown in Fig. 4(b), V_{pz} is flipped from V_{p1} to V_{p2} with respect to a bias voltage $V_{b1} = 6V_b$. The transient resonance lasts for half of an LC period. When V_{pz} reaches V_{p2} , the inductor current returns zero, such that the diode in the conducting path blocks the reverse current and stops the LC resonant current. The presence of these current-steering diodes eliminates the need for current sensing or precise knowledge about the characteristics of any piezoelectric transducer. In the following sub-phases shown in Fig. 4(c)–(g), a series of transient resonances are carried out in sequence, flipping V_{pz} to the zero-voltage direction. It finally stops at V_{p7} . In each of these bias-flip sub-phases, the bias capacitors discharge a little bit during these six sub-phases shown in Fig. 4(b)–(g).

In the sub-phase shown in Fig. 4(h), two switches in the same current steering unit conduct to create a zero-volt bias. V_{pz} is flipped from a positive to a negative value. The equivalent circuit is the same as that in conventional P-SSHI using the zero bias voltage.

In the sub-phase shown in Fig. 4(i), the capacitor array configuration is the same as that in Fig. 4(g), except that the polarity is reversed to produce $V_{b8} = -V_b$. The following sub-phases shown in Fig. 4(j)–(n) are six other transient half-cycle LC resonances to flip V_{pz} to a more negative value number. They are counterpart actions of those illustrated in the sub-phases shown in 4(c)–(g). They use the same bias voltages but with a reversing polarity. In each of these sub-phases, the bias capacitors recharge the same amount of energy as that lost during the former sub-phases shown in Fig. 4(b)–(g). Therefore, the bias capacitors stay energy-neutral, i.e., each bias voltage source maintains the same voltage after the 13

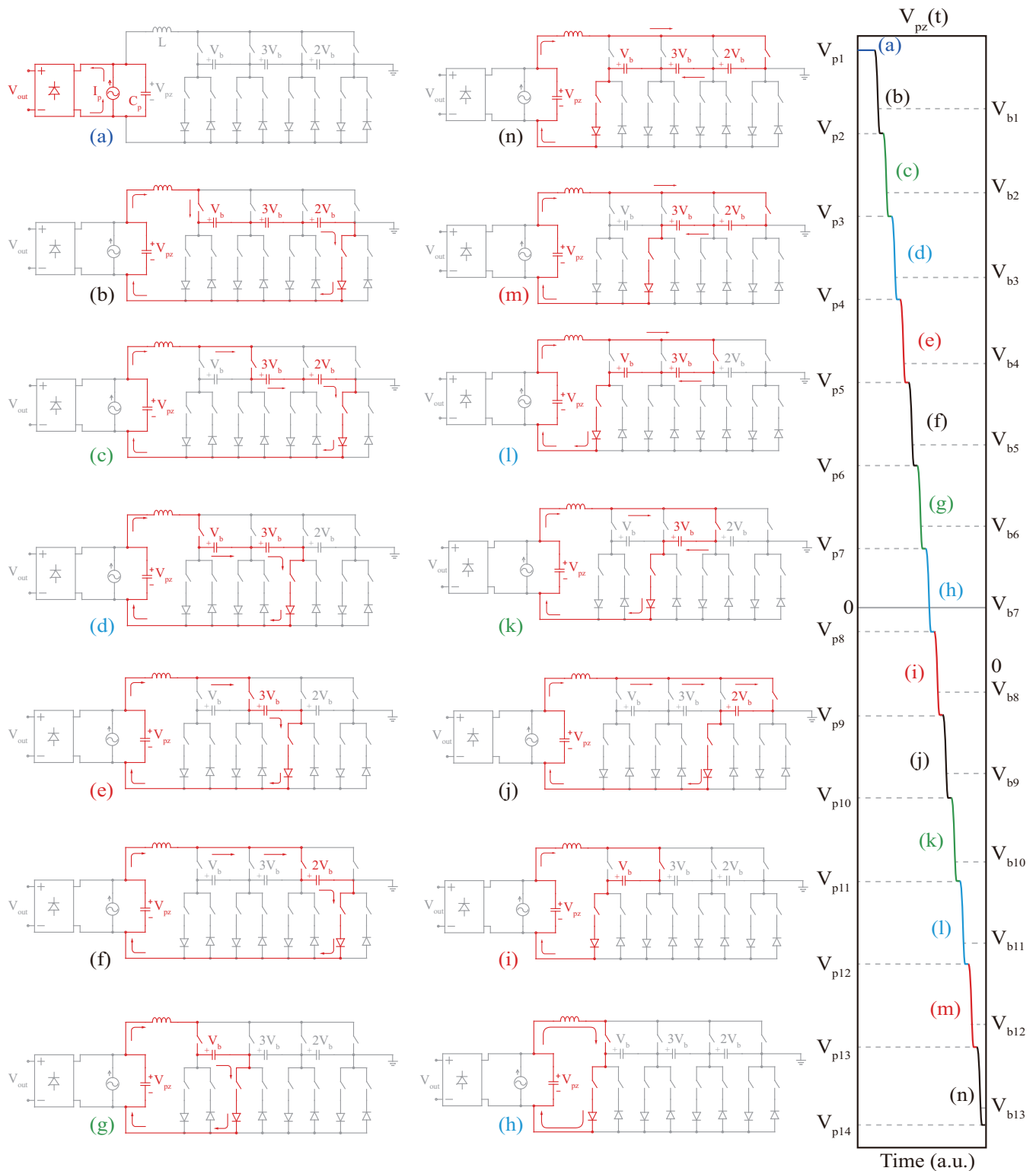


Fig. 4. Different operation modes in a positive to negative voltage flipping action.

actions in one round of bias-flip actions.

After the sub-phase shown in Fig. 4(n), the circuit will enter the open-circuit phase again. i_p charges C_p until $|V_{pz}|$ reaches V_{out} again.

IV. EXPERIMENTAL VALIDATION

In the experiment, a piezoelectric cantilever beam is excited by a shaker (KDJ-20). The piezoelectric electrodes are connected to the prototyped SMBF interface circuit. The dc load is

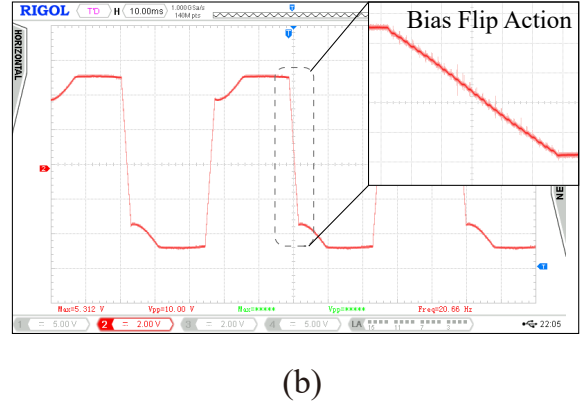
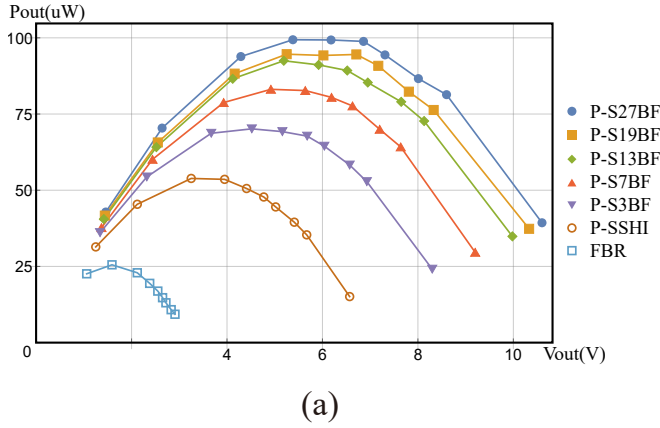


Fig. 5. (a) Harvested power under different bias-flip schemes. The excitation level is equivalent to that generating a 7.82 V V_{pp} open-circuit piezoelectric voltage. (b) The voltage waveform across the PT under the 27 bias-flip scheme (recorded under a load resistance of 200 k Ω).

TABLE II
COMPONENT PARAMETERS IN EXPERIMENT.

Component	Value / Type
C_p	141.6 nF
f_r	20.66 Hz
L	10.06 mH (ESR = 18.4 Ω)
N-channel MOSFET	BSS123W-7-F
P-channel MOSFET	BSS84WQ-7-F
Full bridge rectifier	DB107
Diode	1N4148WS (5 μ A leakage @ 75 V)
Bias capacitors	4.7 μ F (maximum voltage 50 V)
Output capacitor	10 μ F

a variable resistor to measure the harvested power under different rectified voltages. A function generator (DG1032) generates a constant amplitude sinusoidal driving signal. The signal is amplified by a power amplifier and drives the shaker. The function generator also generates a synchronizing square wave indicating the zero crossing point of piezoelectric equivalent current i_p . A microcontroller generates the control sequence of the switch array. Because the topology of a five-capacitor array inclusively contains all those of one- to four-capacitor arrays, we only need one five-capacitor prototype to carry out the comparison. To compare the performance under different numbers of bias-flip actions, we change the control sequence to perform the optimal SMBF control using one to five bias capacitors, respectively. Table II lists the parameters or types of the components used in the experimental prototyped circuit.

A. Results

Fig. 5(a) shows the relationship of output power vs. load voltage in different SMBF harvesting schemes. The FBR can be considered a special case, where the bias-flip number is zero. As the bias-flip number increases, the maximum output power also increases. The ratio of maximum output power is measured as follows

$$P_{FBR} : P_{SSHI} : P_{S3BF} : P_{S7BF} : P_{S13BF} : P_{S19BF} : P_{S27BF} \\ = 1 : 2.11 : 2.74 : 3.25 : 3.62 : 3.70 : 3.89. \quad (2)$$

The output power obtained when implementing a large number (19 or above) of flipping actions is not as high as that predicted by the SMBF theory. One reason is that the SMBF theory has not considered the dielectric loss of the PT and the mechanical damping of the harvesting system. The other reason is the diode voltage drop in the resonant loop was not considered in the original theory as well. The voltage drop appears as an additional bias voltage, so the bias voltage is not optimal when a practical diode is utilized. As the bias-flip number increases, the voltage change before and after each voltage-bias-flip action decreases, making the effect of diodes more non-negligible.

Fig. 5(b) shows the transducer voltage waveform in S27BF using five bias capacitors. The corresponding bias voltages are measured by a multimeter. In the experiment of S27BF, the bias voltages are recorded 0.96 V, 1.19 V, 1.23 V, 0.64 V, and 0.31 V, respectively. The actual bias voltage ratio is 3.09 : 3.83 : 3.6 : 2.06 : 1. Such a ratio is close to the theoretically designed one of 3 : 4 : 4 : 2 : 1. The other voltage ratios under different bias-flip cases are also recorded. The overall error ranges from 1% to 10%. The measurement result validates the self-containment and self-adaptivity of the proposed SMBF implementation under different sets of switched-capacitor arrays.

V. CONCLUSION

This paper proposed a new implementation of parallel-SMBF voltage bias-flip interface circuits for piezoelectric energy harvesting (PEH). The bias-flip interface is constructed by using an optimally arranged and easy-to-drive capacitor array. The capacitor array that consists of five bias capacitors can mostly carry out 27 voltage bias-flip actions by reconstructing and reusing those five capacitors in different operation phases. As an extended and improved design of P-S7BF [11], the proposed circuit topology extracts 289% more power than the benchmarked full-bridge rectifier case. The proposed design makes a new record of the SMBF implementations using high voltage rating discrete components. It is more applicable for

handling the relatively high voltage generated by most low-frequency piezoelectric energy harvesters.

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