

Load-Insensitive Design of Class E Inverter Based on Inequality Constraints

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Abstract--This paper aims at investigating load insensitivity in order to achieve high conversion efficiency across a wide range of loads, departing from the conventional approach of optimizing a classical single-switch resonant converter for a specific load resistance to attain ideal soft switching. This design involves introducing a non-ideal soft switching condition, i.e., partial zero voltage switching, which is mathematically expressed as an inequality constraint. By leveraging the impedance model, the study explores the full design potential of the inverter, allowing for a more balanced trade-off between efficiency and load insensitivity. The experimental results demonstrate the operation of a 1-MHz inverter, maintaining an efficiency over 96% as the load resistance varies within the range of [10, 20] Ω and [10, 60] Ω.

Index Terms--Class E inverter, EIM method, load-insensitive design

I INTRODUCTION

Single-switch converters[1]-[3] have been found extensive application in the areas of radar sensors[4], hybrid vehicle[5] and wireless power transfer[6]-[9]. The remarkable efficiency exhibited by single-switch resonant converters has led to in-depth exploration of various topologies, including Class E[10]-[11] and Class EF[12]-[15]. However, the traditional configuration of single-switch converters commonly demonstrates sensitivity to variations in load conditions. In Class E converters, each specific load resistor corresponds to a fixed combination of X and C_l values, dictated by the equation: ZVS, i.e., zero voltage switching and ZVDS, i.e., zero derivative switching. The alteration of load resistance induces changes in the associated X and C_l values, causing the loss of ZVS and ZVDS, ultimately resulting in a decline in overall efficiency. Therefore, there arises a critical need to develop new methods aimed at alleviating the single-switch converter's sensitivity to load fluctuations, all the while maintaining ZVS to ensure the efficiency.

Previous studies have introduced methods to address the issue of load sensitivity[16]-[20]. However, in the pursuit of achieving load insensitivity, the increase of additional circuit components may give rise to power losses or other problems. It is crucial to assess the applicability and universality of these approaches. This paper proposes a design approach for a single-switch Class-E inverter devised to exhibit insensitivity towards variations in load resistance, while elucidating the trade-off design between efficiency and the range of permissible load resistance. Using EIM[21]-[22], ZVS is represented

by inequality constraint, which would effectively release the design variables. In Section II, by setting up inequalities that render the voltage between the switch terminal during turn-off approaches zero rather than equals to zero (ZVS equality), the goal of load insensitivity Class E is achieved, minimizing the loss of efficiency. In Section III, all X and C_l values satisfying the ZVS inequality were obtained and efficiency-load curves are plotted to visually depict the relationship between the overall efficiency and the range of resistance values. In Section IV, experiments are carried out to verify the realization of ZVS and derive efficiency-load curves to validate the result of simulation.

II LOAD-RESISTANCE INSENSITIVE DESIGN

A. Circuit design variables

The circuit topology of Class E inverter is shown in Fig. 1. It requires a single switch S , and its duty cycle is D . The switching frequency is f and the corresponding angular frequency is ω . L_f is the input choke inductor. C_l is the shunt capacitor across the switch. L_0 resonates with C_0 at f with the additional reactance X , i.e.,

$$X = \omega L_x = \omega L_0 - \frac{1}{\omega C_0} \quad (1)$$

L_x represents the remaining inductive part of the output network. I_{in} represents the input dc current; the output power is calculated as $P_o = I_{o,rms}^2 R$. Note that $I_{o,rms}$ represents RMS value of the output current, and R is the load resistance. The inverter efficiency is defined as $\eta = P_o / (V_{in} I_{in})$.

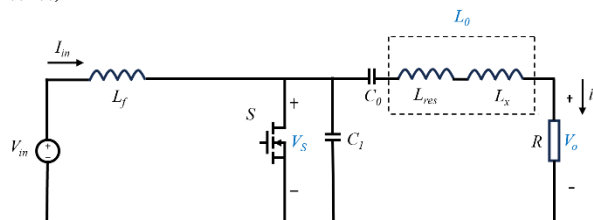


Fig. 1. Classical Class E converter.

B. Resistance insensitive design

With the given duty cycle, X and C_l are regarded as the design variables. The principal focus of this research is to ensure optimal efficiency across a wide load resistance range. In this pursuit, the attainment of ZVS assumes paramount importance, as it represents a crucial criterion conducive to heightened efficiency and diminished power dissipation within single-switch resonant converters. Note that ZVS is represented as an inequality constraint, i.e.,

$$|V_s(t_s)| < \mu \quad (2)$$

is used to release design freedom without significantly sacrificing efficiency, where μ is a small positive number to ensure the attainment of partial ZVS. Fig. 2 illustrates the design flowchart (taking $R \in [10, 60] \Omega$ as an example). Values of X and C_l can vary within a certain range and each cycle begins with an assigned X and C_l . Under the varying load resistance, variables will be represented in matrix form and then matrix manipulation is carried out with input design variables, i.e., V_{in} , f , and D . The utilization of the inequality constraint serves as a mean to evaluate the attainment of ZVS. Any data points failing to satisfy the ZVS constraint are systematically excluded from consideration. Upon conducting the assessment, if it is confirmed that all resistance values falling within the predefined range of 10 to 60 Ω conform to the ZVS inequality, the corresponding values of X and C_l will be documented and preserved as valid parameters for further analysis and application.

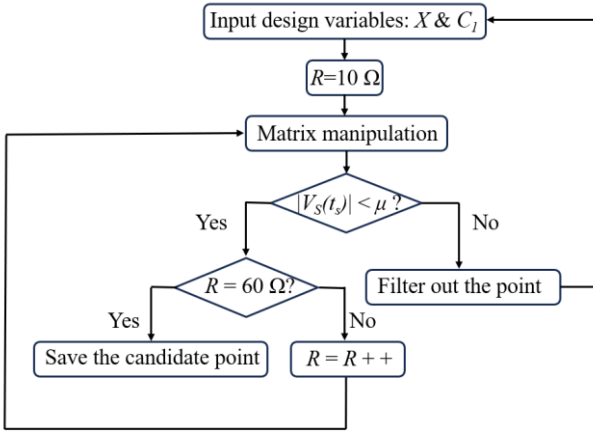


Fig. 2. Resistance insensitive design flowchart ($R \in [10, 60] \Omega$).

This impedance-based method provides an automated method of identifying potential points that adhere to the required constraints by utilizing the inequality constraint specified in equation (2), thereby simplifying the design process.

TABLE I
INPUT DESIGN VARIABLES IN SIMULATION.

f	D	V_{in}	L_f	L_0	μ
1 MHz	0.5	30 V	47 μ H	30 μ H	5 %

When input design variables are determined, i.e., TABLE I, candidate points that ensure ZVS operation when R varies within $[10, 20] \Omega$ and $[10, 60] \Omega$, are filtered out and plotted as shown in Fig. 3. Note that each point represents a combination of X and C_l , and all circuit parameters would be further determined, such as C_0 will be calculated as

$$C_0 = 1/\omega^2 * (L_0 - X/\omega) \quad (3)$$

III EFFICIENCY CURVE UNDER VARYING RESISTANCE

Upon the identification of multiple groups of X and C_l (as depicted in Fig. 3), the next step is the identification of the X and C_l parameters corresponding to the maximal efficiency when $R = 10 \Omega$. Then, following the determination of X and C_l corresponding to the aforementioned configurations, η - R curves are respectively plotted for $R \in [10, 20] \Omega$ and $R \in [10, 60] \Omega$. In the case of $R \in [10, 20] \Omega$, when X is 51.5 Ω and C_l is 1.70 nF, the highest efficiency would achieve 96.8% at $R = 10 \Omega$. Then, the η - R curve ($R \in [10, 20] \Omega$) is plotted when X is 51.5 Ω and C_l is 1.70 nF. When $R \in [10, 60] \Omega$, the highest efficiency at $R = 10 \Omega$ drops to 96.4% and the overall efficiency is lower, compared with the case of $R \in [10, 20] \Omega$.

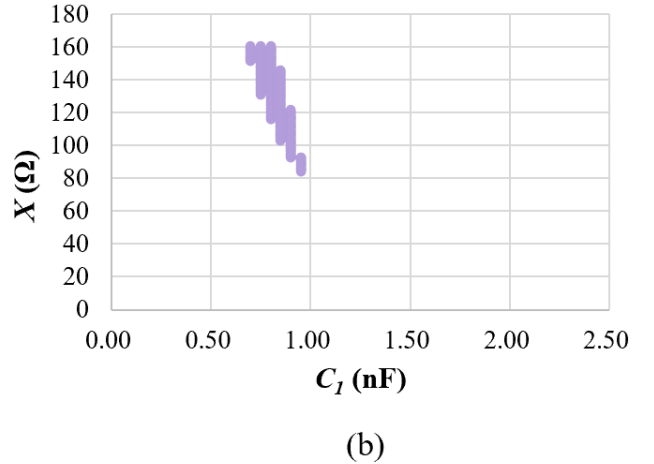
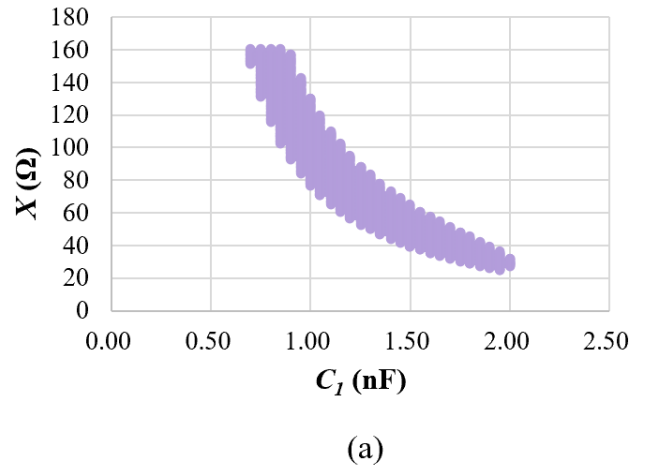


Fig. 3. (a) Candidate points of $R \in [10, 20] \Omega$; (b) Candidate points of $R \in [10, 60] \Omega$.

Fig. 4 shows the η - R curve when $R \in [10, 20] \Omega$ and $[10, 60] \Omega$. In the ideal case (only take the equivalent series resistance into consideration), the efficiency of the Class E inverter achieves 98.2% since ideal ZVS and ZVDS are pursued. Fig. 4 shows that if twice the original resistance is required (i.e., $R \in [10, 20] \Omega$), the efficiency is 96.8%-98.7% when ZVS operation is ensured; if six times the original resistance is required (i.e., $R \in [10, 60] \Omega$), the efficiency is 96.7%-99.0%. It shows that as the variation

range of R expands, there is a noticeable decline in the overall system efficiency. Most previous studies have primarily focused on achieving load insensitivity in converters, yet have not provided a thorough examination of the impact of different ranges of the load resistance on overall efficiency. This paper underscores a trade-off scenario where, if the inverter requires a wider range of load resistance, there is a consequent sacrifice in the overall efficiency.

TABLE II
COMPONENT VALUES OF THE SIMULATION FOR CLASS E INVERTER.
INDUCTANCE UNIT: μH ; CAPACITANCE UNIT: nF .

	L_f	L_0	C_f	C_0
$R \in [10, 20] \Omega$	47	30	1.70	1.16
$R \in [10, 60] \Omega$	47	30	0.95	1.66

Simulations depicted in Fig. 5 serve to validate the performance of the inverter. Due to the implementation of the EIM method, the conventional ZVS equation has been transformed into an inequality, liberating design variables. It is essential to undertake a rigorous validation process to

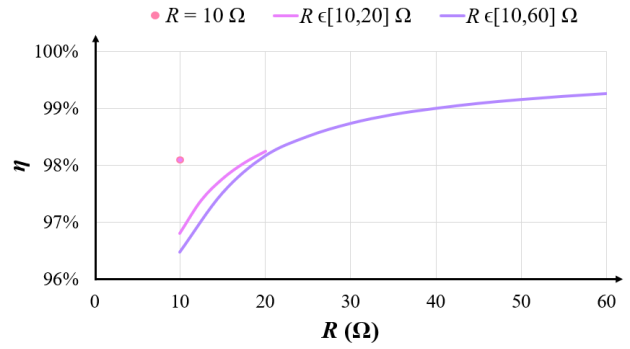


Fig. 4. η - R curve.

ascertain the efficacy of this method in ensuring adherence to ZVS conditions within the circuit topology, thereby guaranteeing the attainment of high operational efficiency. Specifically, Fig. 5 (a) presents the waveform v_S under varying load resistances of 10Ω , 15Ω , and 20Ω . The attainment of ZVS is confirmed across the range of load resistances within $[10, 20] \Omega$. Fig. 5 (b) illustrates the v_S waveform when $R = 10 \Omega$, 30Ω , and 60Ω . It is confirmed that ZVS is attained when the load resistance varies within the range of $[10, 60] \Omega$. Thus, the designed inverters demonstrate consistent ZVS operation across a wide range of load resistances, ensuring efficient performance under varying conditions.

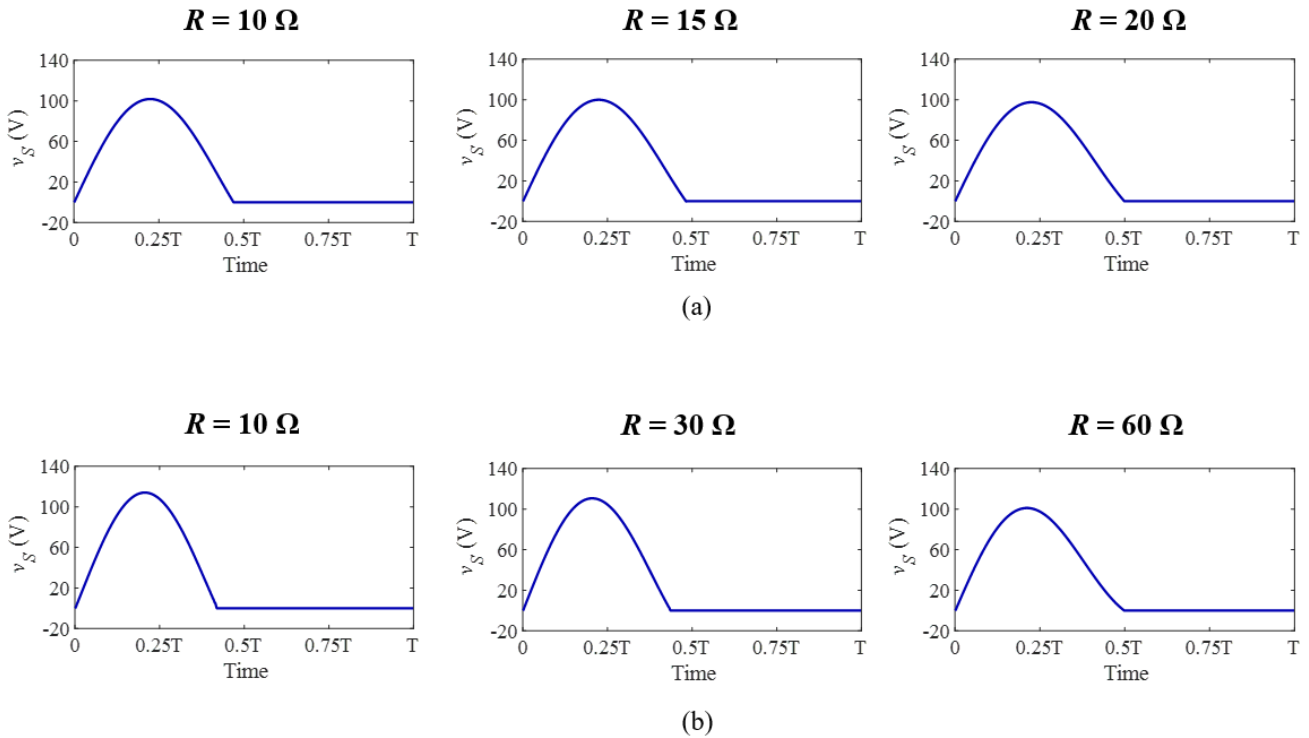


Fig. 5. Waveform of switch voltage v_S . (a) $R \in [10, 20] \Omega$. (b) $R \in [10, 60] \Omega$.

IV EXPERIMENTAL VERIFICATION

The experiment platform is built (as depicted in Fig. 6) to verify the simulation of the η - R curve (i.e., Fig. 4). Among numerous X and C_I values that meet the ZVS, each parameter set (i.e., X and C_I) corresponds to a different efficiency at a fixed load resistance. To confirm the simulation, X and C_I are determined to enable the circuit to achieve the highest efficiency at $R = 10 \Omega$, when $R \in [10, 20] \Omega$ and $R \in [10, 60] \Omega$, respectively. Efficiency testing is conducted on three points i.e., $R = 10 \Omega$, 15Ω , and 20Ω when $R \in [10, 20] \Omega$; And six points, i.e., $R = 10 \Omega$, 20Ω , 30Ω , 40Ω , 50Ω , 60Ω are tested, when $R \in [10, 60] \Omega$. Moreover, the efficiency of the theoretical optimum point is evaluated at $R = 10 \Omega$. During the test, efficiency is calculated by the definition, i.e., $\eta = P_o / (V_{in} I_{in})$, and the voltage between the switch (i.e., v_s) is measured.

Fig. 7 illustrates that all examined data points ensure the attainment of ZVS operation. Although the EIM method releases design variables, it does not affect the overall satisfaction of ZVS within the circuit, thereby achieving high efficiency. Therefore, the employment of the EIM method not only guarantees ZVS operation but also facilitates the exploration of Class E inverter designs that exhibit insensitivity to load variations.

For load resistances within the range $[10, 20] \Omega$, the efficiency ranges from 95.4% to 97.9%. Extending the load resistance range to $[10, 60] \Omega$ results in efficiency variations spanning from 89.5% to 98.8%. Specifically, at $R = 10 \Omega$, the inverter efficiency is measured at 97.4%.

As depicted in Figure 8, there is an observable trend where the overall efficiency experiences a decrease with

an expansion of the load resistance range. In order to achieve a wider ZVS load range, it requires a trade-off design in terms of efficiency and the load range.

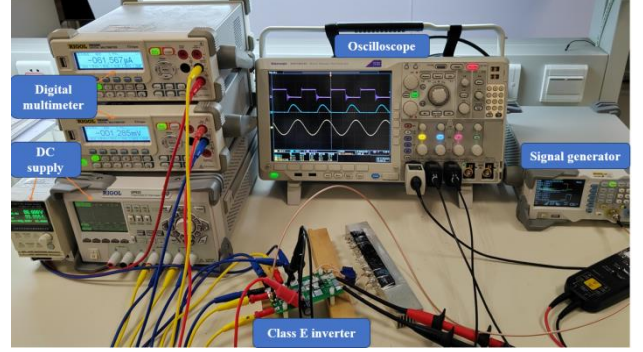


Fig. 6. Experiment platform.

V CONCLUSIONS

This paper explores a load resistance insensitive design and shows the trade-off between system efficiency and the range of the load resistance. By employing EIM, a partial ZVS inequality constraint is utilized to reduce the switch loss, and the design variables are released. The candidates that ensure the ZVS operation are filtered out and plotted. The combination of X and C_I that maximizes the overall efficiency at $R = 10 \Omega$ is selected, and the corresponding efficiency-load curves are illustrated.

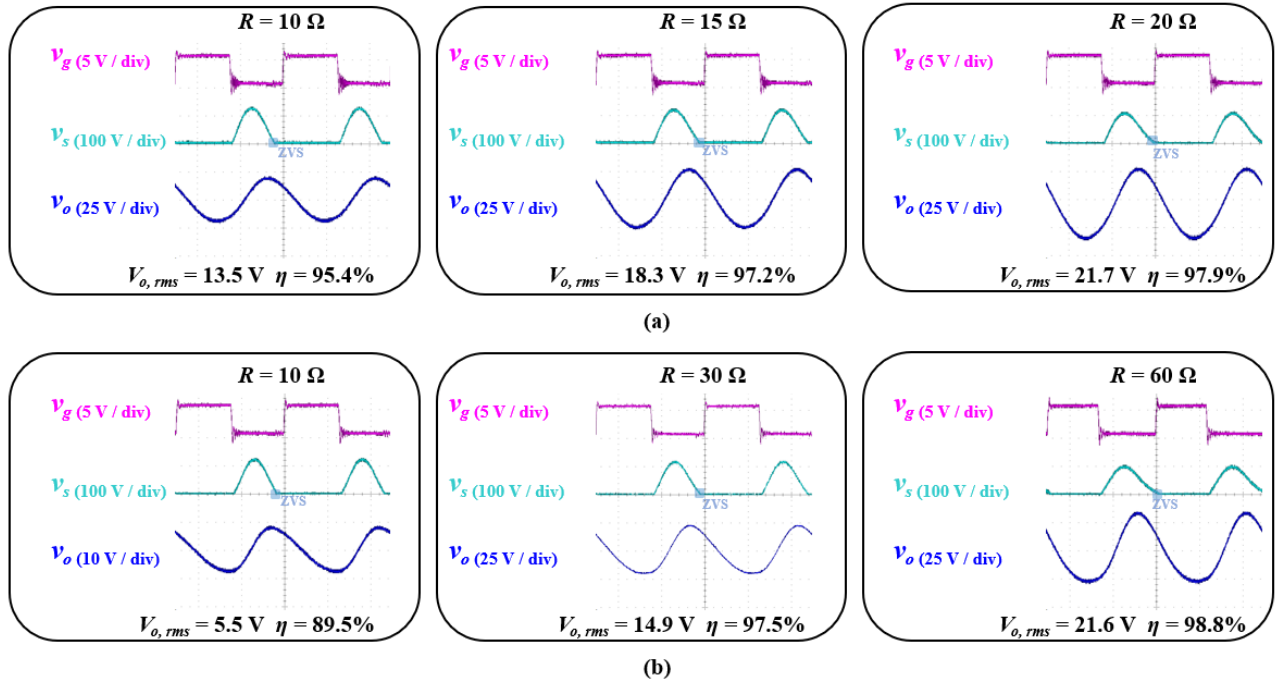


Fig. 7. Waveform of V_g , V_s and $V_{o,rms}$. (a) $R \in [10, 20] \Omega$. (b) $R \in [10, 60] \Omega$.

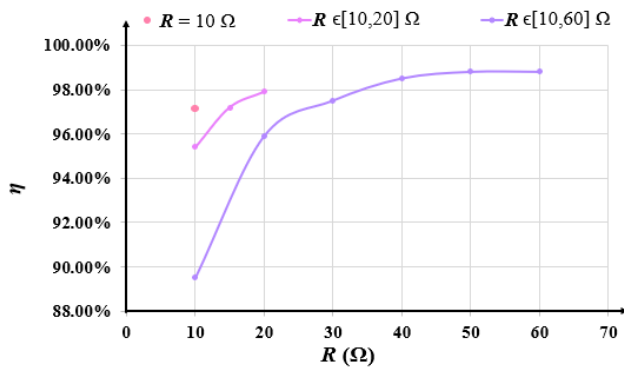


Fig. 8. η - R curve in the experiment.

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