

Letters

Load-Impedance-Insensitive Design of High-Efficiency Class EF Inverters

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Abstract—This letter develops a high-efficiency Class EF inverter under ultrawide load impedance variation. The inequality constraints are introduced to fully release the design potential when the partial zero voltage switching operation serves as the primary goal. The load-reactance insensitivity is discussed based on the inverter's robustness under circuit parameter variation. The switch voltage stress is also considered for the final tradeoff design. In the experiment, when the load resistance varies in [15, 40] Ω and load reactance varies [−17, 17] Ω , a 1-MHz inverter is built and shown to operate normally with efficiency above 92%.

Index Terms—Load-reactance insensitive, multiple inequality constraints, resonant converter, tradeoff design.

I. INTRODUCTION

SINGLE-SWITCH resonant converters have been widely used in high-frequency operating scenarios (i.e., plasma generation, wireless power transfer, and medical devices) due to the simple configuration, zero voltage switching (ZVS), and high operating efficiency. Many single-switch converters have been proposed, such as Class E, Class F, and their derivatives (i.e., Class Φ_2 and the Class EF family) [1], [2], [3]. The conventional design of single-switch converter is usually sensitive to the load variation. For example, the optimal operation of a Class E inverter only happens for a specific load resistance. The corresponding system efficiency would drop significantly as the load resistance varies.

In order to ensure the load-insensitive operation, several methods are proposed in the previous works. Impedance compression

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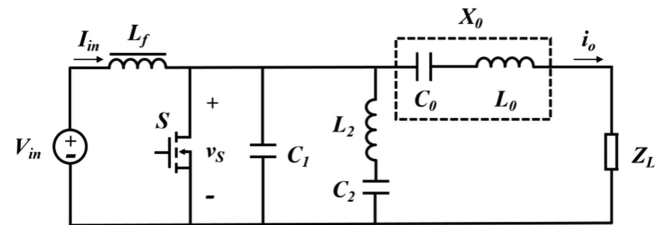


Fig. 1. Topology of a Class EF inverter.

techniques are effective in reducing the impedance fluctuations. Using an auxiliary network, load insensitivity is achieved regardless of the converter topology design [4], [5]. From the topological point of view, the load-resistance-insensitive designs have been broadly evaluated in [6], [7], [8], [9], [10], [11], [12], and [13]. However, a real application usually needs to consider both resistance and reactance variation. The significant deviation of the load reactance, such as the reflected varying load in the wireless power transfer system, would affect the resonance, ZVS operation, and even fails the converter. Currently, load-reactance-insensitive operation is derived and analyzed for Class DE converter based on the cooperation of two single-end inverters [14]. Using a single-switch topology, Arteaga et al. [15] gave boundaries of the equivalent inverter output voltage that satisfies the temperature constraints. Complicated data gathering and training are required to obtain the waveform for wide-load-reactance design [16].

This letter is devoted to a load-impedance-insensitive design for a single-switch Class EF inverter. By pursuing partially ZVS operation, the potential design variables are fully released. It starts from a fixed-reactance and varied-resistance scenario. Several inequality constraints are defined to generate a tank of candidates. The inverter robustness to the series reactance variation is utilized to search for load-reactance-insensitive design. The switch peak voltage is then included to make a final tradeoff solution. Experiments have been implemented to verify the load-impedance-insensitive operation.

II. LOAD-IMPEDANCE-INSENSITIVE INVERTER

A. Design Variables

Fig. 1 shows a Class EF inverter. It includes a single transistor S , whose duty cycle is D and switching frequency is f_s . The

input inductor L_f serves as an RF choke. C_1 is a shunt capacitor that absorbs the switch junction capacitance. At f_s , L_0 and C_0 resonates with additional reactance X_0

$$X_0 = \omega_s L_0 - 1/(\omega_s C_0). \quad (1)$$

The shunt tank L_2 and C_2 would resonate at f_2

$$f_2 = 1/(2\pi\sqrt{L_2 C_2}). \quad (2)$$

When the switch peak voltage is $v_{s,\text{peak}}$, it could be normalized with respect to the input voltage V_{in} , i.e.

$$\beta = v_{s,\text{peak}}/V_{\text{in}}. \quad (3)$$

Given the load impedance $Z_L (= R_L + jX_L)$, when the output RMS current is $I_{o,\text{rms}}$, the overall output power is $P_o = I_{o,\text{rms}}^2 R_L$. Since L_f is large, the input current is dominated by its dc component, I_{in} . Thus, the inverter efficiency is defined as $\eta = P_o/(V_{\text{in}} I_{\text{in}})$.

In Fig. 1, there are five resonant components to design an inverter. Since the inductors are not convenient for continuous tuning, L_2 and L_0 could be predefined and fixed. Given the duty cycle D , there are mainly three design variables, i.e., C_0 , C_1 , and C_2 . Based on (1) and (2), f_2 , C_1 , and X_0 would serve as the direct design variables.

B. Impedance-Insensitive Design

In this letter, the primary goal is to ensure high efficiency under all loading scenarios. Note that a partial ZVS operation (i.e., slightly losing ZVS) would release the design freedoms without significantly increasing the switching losses. Meanwhile, the secondary goal is to ensure the output stability without regulation instead of an ideal constant output current. Considering these basic demands, the proposed Class EF inverter needs to meet the following inequality constraints:

$$\begin{cases} |v_S(t_s)| < \epsilon \\ (I_{o,\text{max}} - I_{o,\text{min}})/(I_{o,\text{max}} + I_{o,\text{min}}) < \sigma \\ P_o > P_{\text{set}} \end{cases} \quad (4)$$

where ϵ and σ are small positive numbers, P_{set} represents the minimum target power, and $I_{o,\text{max}}$ and $I_{o,\text{min}}$ represent the maximum and minimum RMS current. Note that ϵ , σ , and P_{set} are determined based on practical demands.

Fig. 2 illustrates the design flowchart. With the three fundamental inputs, i.e., the chosen topology, fixed components, and design variables, the impedance model is built for each circuit component. Impedance-based methods are employed to solve the target state variables [10]. By describing each circuit component as an impedance matrix, a single KCL equation is given. The target state variables are solved and represented in time domain. The Z_L -insensitive design would start from the R_L -insensitive condition. For example, when $f_s = 1$ MHz, $D = 0.5$, $V_{\text{in}} = 60$ V, $L_f = 47$ μH , $L_0 = 30$ μH , and $L_2 = 5$ μH , the initial target is to find the domains for the three design variables (i.e., f_2 , C_1 , and X_0) when $X_L = 0$ and $R_L \in [15, 40]$ Ω . Note that the frequency-independent parameters are used for circuit design, and 1 MHz is just an example frequency.

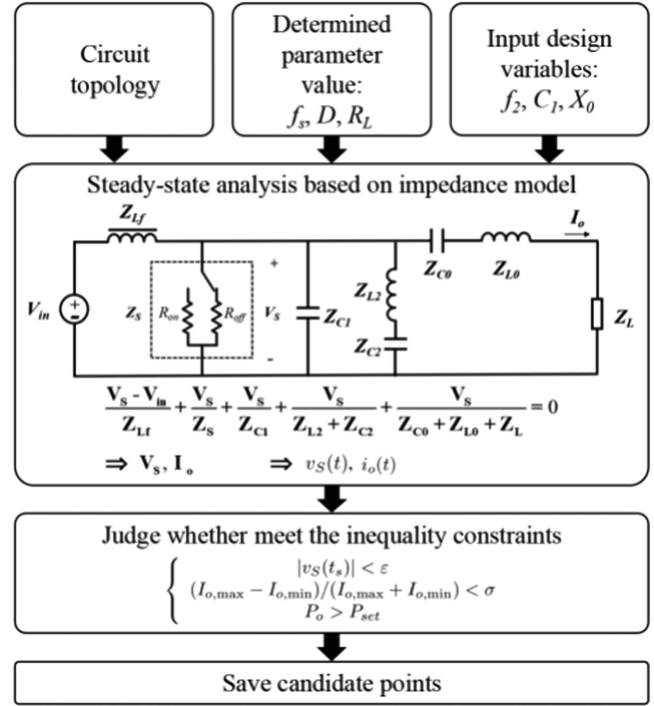


Fig. 2. Flowchart of the circuit design.

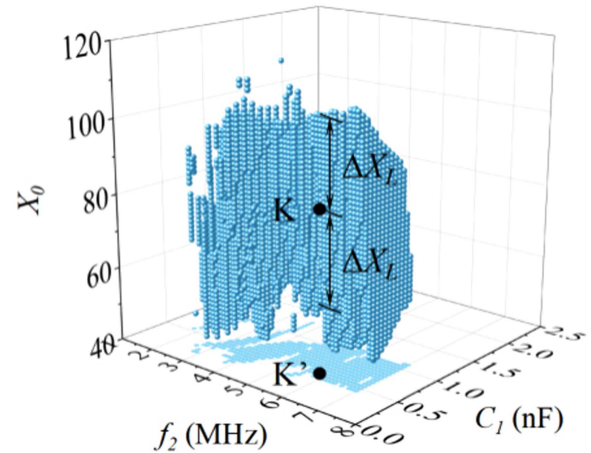


Fig. 3. Candidate points.

With the help of circuit simulation or analytical-model-based calculation, the inequality constraints of (4) are used to find the solution. An example case would use $\epsilon = 5\%$, $\sigma = 10\%$, and $P_{\text{set}} = 18$ W in (4), and Fig. 3 shows the candidate points. Note that any point represents a specific combination of the three design variables, i.e., f_2 , C_1 , and X_0 . Based on the inequality constraints, the released restriction would help define a large number of candidates, which actually fully explores the design potentials. By modifying the initial demand, the insensitivity design would also start from a fixed-resistance varied-reactance case.

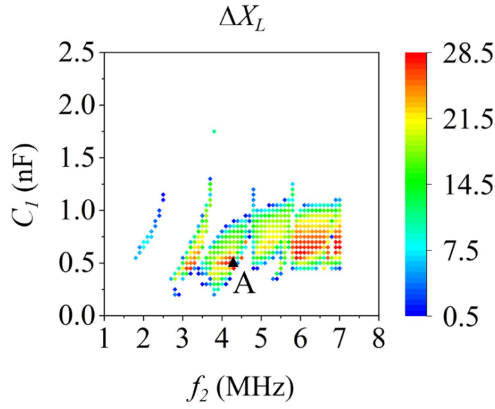


Fig. 4. Load reactance variation for different f_2 and C_1 .

The surviving candidates of Fig. 3 need to be further filtered out by considering load reactance variation. Note that the resistance variation has been included. The z-axis of Fig. 3 represents the series reactance X_0 , which is actually in series with Z_L in Fig. 1. The varied X_L could be viewed as a varied X_0 . For example, in Fig. 3, a specific Point K is defined in the bottom plane. Point K could be viewed as the projection of the candidates with the same f_2 and C_1 in the 3-D map. Among these points, the inverter's objectives are robust under a wide X_0 , and X_0 is usually allowed to vary in a continuous range, i.e., $X_0 \in [X_{0,\min}, X_{0,\max}]$. A variation range is defined as

$$\Delta X_0 = (X_{0,\max} - X_{0,\min})/2. \quad (5)$$

When the final design is selected at K in Fig. 3, whose X_0 is right in the middle of $[X_{0,\min}, X_{0,\max}]$, the inverter operating at K would show to be insensitive to X_0 variation when $X_L = 0$. It also means the inverter would be insensitive to X_L for a fixed X_0 . For the specific f_2 and C_1 , its allowable load reactance variation is defined as $\Delta X_L (= \Delta X_0)$.

Fig. 3, represented by f_2 , C_1 , and X_0 , could be converted to Fig. 4, presented f_2 , C_1 , and ΔX_L . ΔX_L is denoted by the color strength, and $\Delta X_L \in [0.6, 28.3]$. Point A could achieve the largest ΔX_L . Once Point A is selected, its ΔX_L needs to combine with its corresponding $[X_{0,\min}, X_{0,\max}]$ to obtain the required X_0 , i.e., $X_0 = X_{0,\min} + \Delta X_L = X_{0,\max} - \Delta X_L$. Finally, the final design point can be located in Fig. 3. Using this design, the load impedance variation will not jump out the domain defined by (4).

When three direct design variables are determined by Point A, all the rest capacitors are designed based on (1), (2), and an example design is given in Table I. A circuit simulation is carried out to test the inverter performance. In Fig. 5, the transistor voltage is recorded for different load impedance. When the load becomes capacitive with $X_L = -28.3 \Omega$ or inductive with $X_L = 28.3 \Omega$, the transistor waveform would still ensure low switching losses, and the maximum β is 5.4.

TABLE I
INVERTER PARAMETERS AND PERFORMANCE

Point	L_f	L_0	L_2	C_0	C_1	C_2	ΔX_L	β
A	47	30	5	1.38	0.5	0.27	28.3	5.4
B	47	30	5	1.24	0.95	0.41	3.8	3.5
C	47	30	5	1.35	0.7	0.47	17	3.7

Inductance unit: μH ; capacitance unit: nF; impedance unit: Ω

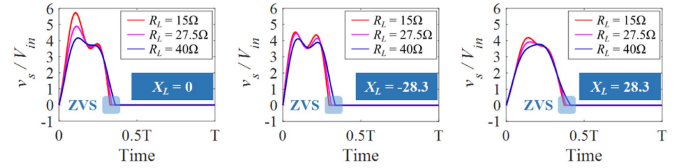


Fig. 5. v_s of Point A.

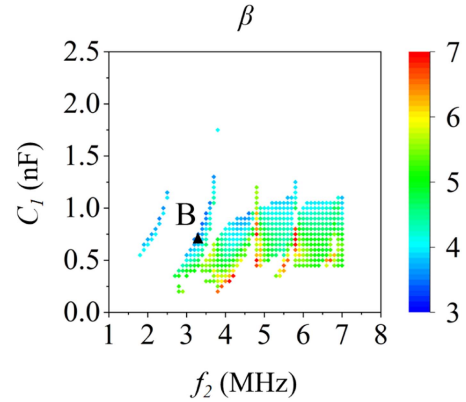


Fig. 6. Peak voltage ratio β for different f_2 and C_1 .

C. Tradeoff Design

The inequality constraints generate large number of points in Fig. 3, and the maximum load reactance range serves as the primary goal for the selection of Point A. It is meaningful to ensure that the designed inverter would not significantly sacrifice the conventional objectives, such as small β . Based on the same candidates of Fig. 4, the corresponding β would be evaluated in Fig. 6. Since each specific design point would define a ΔX_L and β , Fig. 7 directly correlates these two objectives.

In Fig. 7, Points A and B represent the optimum solution for maximum ΔX_L and minimum β , respectively. Point A in Fig. 4 has the largest ΔX_L and a high voltage stress ($\beta = 5.4$). Point B actually tries to minimize β , which is reduced to 3.5. The bottom points of Fig. 7 (within the blue shade area) would be used to select other tradeoff solutions when considering β and ΔX_L , such as Point C. Their parameters are designed in Table I. Fig. 8 shows the voltage waveform of the transistor at different load impedance, which justified the reduced β compared with Fig. 5.

The proposed method is universally applicable to be extended to various topologies. Following the similar design process of Fig. 2, i.e., changing the input topology, design points of Class E inverter are found. Bottom points that considers β and ΔX_L are

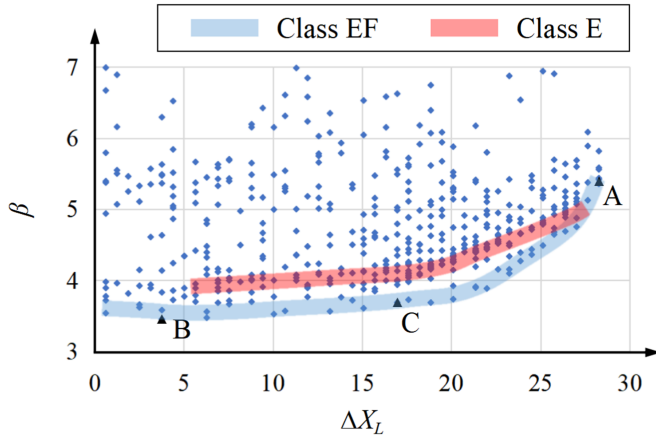


Fig. 7. Tradeoff design of various inverters.

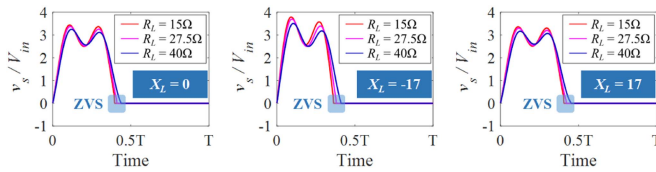
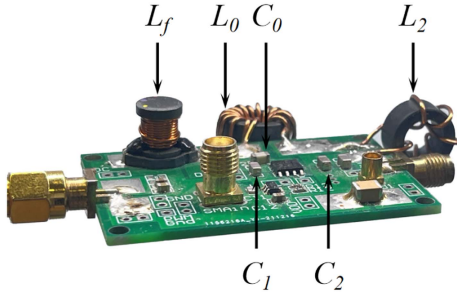

 Fig. 8. v_s of Point C.


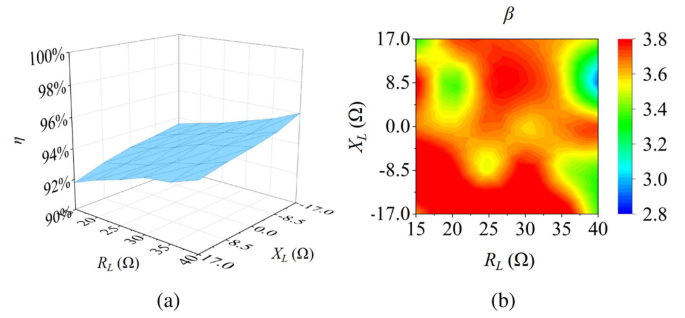
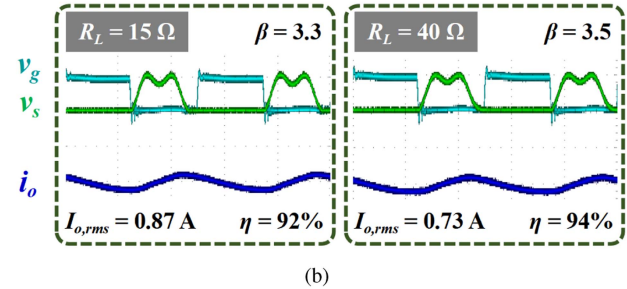
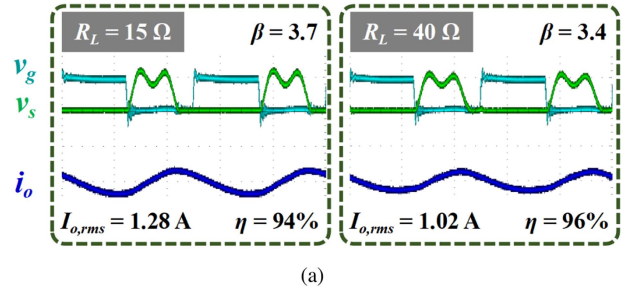
Fig. 9. Prototype inverter.

given in Fig. 7 (within the red shade area). It shows that Class EF inverter outperforms lower β compared with Class E inverter, within the same range of load reactance.

III. EXPERIMENTAL VERIFICATION

A 1-MHz Class EF inverter is implemented in Fig. 9. During the test, the load resistance R_L is manually tuned by a real resistor, and the load reactance X_L is equivalently tuned by changing C_0 .

When $R_L \in [15, 40] \Omega$ and $X_L \in [-17, 17] \Omega$, the inverter efficiency is measured, as shown in Fig. 10(a). Its efficiency is maintained higher than 92% with a peak value at 96%. The peak voltage factor is shown in Fig. 10(b), which is consistent with the design objective. Note that β is affected by the overall filtering effects. The shunt LC branch (i.e., L_2 and C_2) and the series LC branch (i.e., L_0 and C_0), together with the input dc filter and the transistor shunt capacitor, contribute to shaping the transistor waveform. β is mainly determined by the ratio of


 Fig. 10. Inverter performance under impedance variation. (a) η . (b) β .

 Fig. 11. Waveform of Point C: v_g (5 V/div), v_s (200 V/div), and i_o (5 A/div). (a) $X_L = -17 \Omega$. (b) $X_L = 17 \Omega$.

fundamental components (mainly affected by series branch) and third-harmonic components (mainly affected by shunt branch). More details are given in Fig. 11 for extreme load impedance, i.e., $Z_L = 15 \pm j17 \Omega$ and $40 \pm j17 \Omega$. The loss of ZVS operation is not significant due to the small ϵ . Due to the second inequality constraints of (4), the output current is not significantly affected by the load resistance but would be affected by the load reactance. In this letter, almost all the design potentials are reserved to ensure Z_L -insensitive ZVS operation instead of Z_L -insensitive output. An inverter is also designed at Point A for maximum $\Delta X_L (= 28 \Omega)$. Compared with Fig. 11, the waveform of Fig. 12 clearly shows the increased β .

Table II compares the load-insensitive design for a single-switch resonant converter. Note that N represents the number of inductors. It shows most of the previous papers only discuss the resistance variation (i.e., zero or very small ΔX_L). Papers with no discussion on the load-reactance-insensitive design are marked as $\Delta X_L = 0$. The prototype inverter would ensure the high-efficiency operation under ultrawide impedance (considering both R_L and X_L).

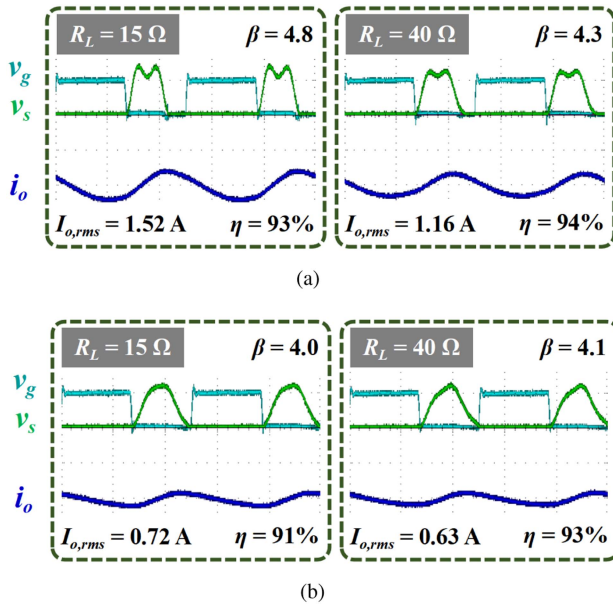


Fig. 12. Waveform of Point A: v_g (5 V/div), v_s (200 V/div), and i_o (5 A/div). (a) $X_L = -28 \Omega$. (b) $X_L = 28 \Omega$.

TABLE II

COMPARISON OF THE SINGLE-SWITCH LOAD-INSENSITIVE INVERTER DESIGN

Ref	f_s (MHz)	R_L (Ω)	ΔX_L (Ω)	η	β_{max}	P_o (W)	N
[1]	13.56	[0.56,6]	0	[-,90%]	2.3	150	3
[2]	27.12	[25,250]	0	[56%,90%]	2.2	25	3
[3]	13.56	[30,70]	0	-	2	25	3
[5]	13.56	50	4	[88%,95%]	2	350	5
[10]	1	5	2.3	[96%,97%]	3.3	25	2
[10]	1	[5,15]	0	[90%,97%]	3	20	3
[11]	6.78	10	0	94%	3	-	2
[17]	6.78	[10,100]	0	[87%,95%]	4	30	3
Point A	1	[15,40]	28	[91%,94%]	4.8	18	3
Point C	1	[15,40]	17	[92%,96%]	3.7	18	3

Frequency unit: MHz; impedance unit: Ω ; power unit: W

IV. CONCLUSION

This letter fully explore the capability of a Class EF inverter to achieve load-impedance-insensitive ZVS operation. In order to release the design freedom, the system basic objectives (i.e., partial ZVS operation, stable output current, and minimum power) are mathematically defined as three inequality constraints. The generated design candidates for load-resistance-insensitive operation are then filtered out by considering the varied reactance and switch peak voltage. A tradeoff design is verified in the experiment to show the high-efficiency ($>92\%$) operation under wide impedance variation.

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